May 10,2023

Senodia
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SH5001 DATASHEET

6-Axis IMU

Package:14-Pin LGA

Dimension:3.0×2.5×0.99mm³

Document Revision: 1.0

1 Basic Descriptions

1.1 SH5001

SH5001 is a highly integrated and low power 6-axis inertial measurement unit (IMU) that combines both 16-bit triaxial acceleration and angular rate measurement in one chip. The device features on-chip motion-triggered interrupts and on-chip FIFO. Specially, SH5001 contains configurable secondary digital interface which can act as I^2C master interface or SPI slave interface for OIS application. The device integrates:

- 16-bit digital 3-axis accelerometer with $\pm2g$, $\pm4g$, $\pm8g$ and $\pm16g$ range

- 16-bit digital 3-axis gyroscope with $\pm125dps$, $\pm250dps$, $\pm500dps$, $\pm1000dps$, $\pm2000dps$ range

1.2 Features and Benefits

- Compact and small size, 14-Pin LGA package with 3.0×2.5 mm^2 footprint

- Wide operating temperature range: -40°C - 85°C

- Wide power supply range: VDD 1.71V-3.60V and independent VDDIO 1.71V-3.60V

- Configurable secondary digital interface for AUX devices

- User-programmable low-pass filter for both accelerometer and gyroscope

- User-programmable interrupts

- On-chip digital output temperature sensor

- Configurable secondary digital interface for AUX devices

- 2kB on-chip FIFO for accelerometer, gyroscope, temperature and AUX sensor data

- 2 independent programmable I/O pins for interrupt

- RoHS compliant, halogen and lead free

1.3 Applications

- Smart phones and tablets

- Optical and electronic image stabilization

- Augmented / Virtual reality

- Smart watches,wristbands and fitness trackers

- Smart TV

- Motion-enabled game and application framework

- Attitude monitoring

- Smart toys

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2 Functional Diagram

Figure 1: Functional diagram of the device

3 SH5001 Specifications

All parameters specified are tested at VDD=3.0V and T=25°C, unless otherwise noted.

3.1 Gyroscope Specifications

Table 1: Gyroscope specifications

Parameter	Condition	Min	Typ	Max	Unit
Full Scale Range	Selectable via serial digital interface		$\pm$ 125		dps
			$\pm$ 250		dps
			$\pm$ 500		dps
			$\pm$ 1000		dps
			$\pm$ 2000		dps
Sensitivity	Selectable via serial digital interface		262		LSB/dps
			131		LSB/dps
			65.5		LSB/dps
			32.8		LSB/dps
			16.4		LSB/dps
Nonlinearity	Best fit straight line		$\pm$ 0.2		$\%FS$
Cross-axis Sensitivity			$\pm$ 0.5		$\%$
Sensitivity Temperature Drift	-40°C - 85°C		$\pm$ 0.02		$\%/^oC$
Zero Rate Temperature Drift	-40°C - 85°C		$\pm$ 0.04		$dps/^oC$
Zero Rate Offset			$\pm$ 1.0		dps
Output Noise Density			5.1		$mdps/\sqrt{Hz}$
Output Data Rate	Selectable via serial digital interface		125		Hz
			250		Hz
			500		Hz
			1000		Hz
			2000		Hz
			4000		Hz
			8000		Hz
			16000		Hz
			32000		Hz

3.2 Accelerometer Specifications

Table 2: Accelerometer specifications

Parameter	Condition	Min	Typ	Max	Unit
Full Scale Range	Selectable via serial digital interface		$\pm$ 2		g
			$\pm$ 4		g
			$\pm$ 8		g
			$\pm$ 16		g
Sensitivity	Selectable via serial digital interface		16384		LSB/g
			8192		LSB/g
			4096		LSB/g
			2048		LSB/g
Nonlinearity	Best fit straight line		$\pm$ 0.5		$\%FS$
Cross-axis Sensitivity			$\pm$ 0.5		$\%$
Sensitivity Temperature Drift	-40°C - 85°C		$\pm$ 0.01		$\%/^oC$
Zero_g Temperature Drift	-40°C - 85°C		$\pm$ 1.0		$mg/^oC$
Zero_Offset			$\pm$ 50		mg
Output Noise Density			150		$\mu g/\sqrt{Hz}$
Output Data Rate	Selectable via serial digital interface		125		Hz
			250		Hz
			500		Hz
			1000		Hz
			2000		Hz
			4000		Hz
			8000		Hz

3.3 Temperature Sensor Specifications

Table 3: Temperature sensor specifications

Parameter	Condition	Min	Typ	Max	Unit
Operating Range		-40		85	^oC
25 ^{o}C Output			2215 [1]		LSB
Resolution [2]			12		bit
Sensitivity			14		$LSB/^oC$
Sensitivity Error		-1		1	$\%$
Output Data Rate	Selectable via serial digital interface		537		Hz
			269		Hz
			134		Hz
			67		Hz

1. This is just an empirical value. Using the factory calibrated room temperature offset is recommended for calculating the temperature value.
2. The temperature sensor reading is a 12-bit unsigned value. Refer to 5.2 for further information on how to convert the readings to degrees centigrade.

3.4 Power Modes

Table 4: Power modes

Mode	Condition	Min	Typ	Max	Unit
Normal	High performance		1590		μA
Acc Only	Accel only		194		μA
Acc Low Power	Acc Low Power		79		μA
Gyro only	Gyro only		1500		μA
Power Down			8.8		μA

The device has two distinct power supply pins:

- VDD is the main power supply.

- VDDIO is seperate power supply pin for the interface and auxiliary interface.

There are no limitations with the voltage level applied to the VDD and VDDIO pins,as long as it lies within the voltage operating range.

The device can be completely switched off (VDD=VDDIO=0), all interface pins(SCK/SDA/SENB/SDO) must be kept close to GND.

The device is not allowed switched off(VDD=0) while keeping the VDDIO supply.

The device will be reset when the supply voltage applied to VDD, VDDIO delayed by more than 10ms after VDD.

No constraints exists for the slow-rate of the voltage applied to the VDD and VDDIO pins.

3.5 Electrical Characteristics

Table 5: Electrical characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
VDD	Supply Voltage		1.71	1.80	3.60	V
VDDIO	Supply Voltage I/O		1.71	1.80	3.60	V
Idd	Supply Current	VDD=3.0V		1.70		mA
V_{IL}	Digital Low-level Input Voltage				0.3VDDIO	V
V_{IH}	Digital High-level Input Voltage		0.7VDDIO			V
V_{OL}	Digital Low-level Output Voltage				0.2	V
V_{OH}	Digital High-level Output Voltage		VDDIO-0.2			V

3.6 Digital Interface Characteristics

3.6.1 Serial Peripheral Interface (SPI)

Subject to general operation conditions like VDD, operating temperature and PCB design.

Table 6: SPI interface characteristics

Symbol	Parameter	Min	Max	Unit
t_{sck}	SPI Clock Period	100	1000	ns
f_{sck}	SPI Frequency	1	10	MHz
t_{sucsb}	CSB Setup Time	20		ns
t_{hcsb}	CSB Hold Time	20		ns
t_{susdi}	SDI Setup Time	20		ns
t_{hsdi}	SDI Sold Time	20		ns
t_{vdsdo}	SDO Valid Time		30	ns
t_{hsdo}	SDO Hold Time	20		ns
t_{dissdo}	SDO Disable Time		10	ns
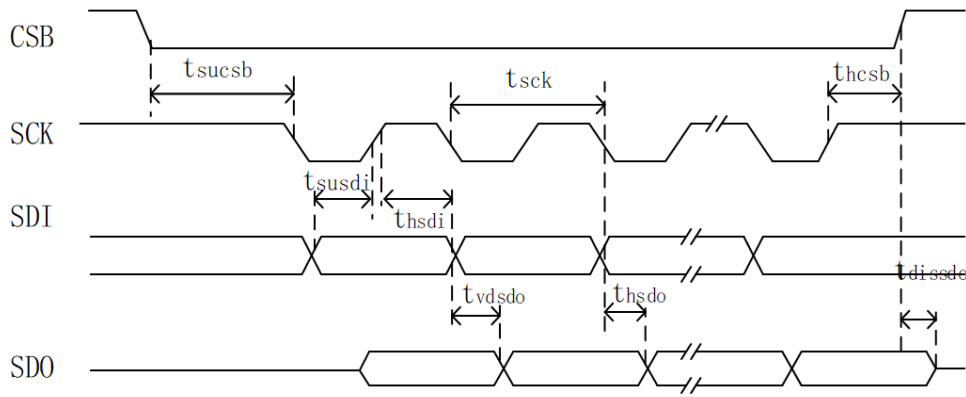
Figure 2: SPI timing diagram

3.6.2 Inter-Integrated Circuit (I^{2}C)

Subject to general operation conditions like VDD, operating temperature and PCB design.

Table 7: I^{2}C interface characteristics

Symbol	Parameter	Min	Max	Unit
f_{sck}	I^{2}C Frequency		1	MHz
t_{low}	I^{2}C Clock Low Time	0.5		μs
t_{high}	I^{2}C Clock High Time	0.5		μs
t_{sudat}	SDA Data Setup Time	150		ns
t_{hdat}	SDA Data Hold Time	0	1	μs
t_{sursta}	Repeat Start Condition Setup Time	0.5		μs
t_{hsta}	Start Condition Hold Time	0.5		μs
t_{susp}	Stop Condition Setup Time	0.5		μs
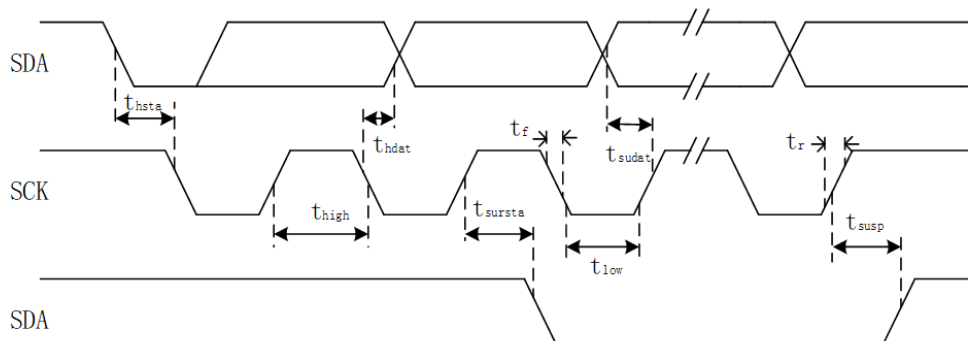
Figure 3: I^{2}C timing diagram

3.7   Absolute Maximum Ratings

Table 8: Absolute maximum ratings

Parameter	Rating	Unit
Voltage at Supply Pin	-0.6 - 3.6	V
Operating Temperature Range	-40 - 85	^oC
Storage Temperature Range	-40 - 105	^oC
ESD (HBM)	±2000	V
ESD (MM)	±200	V
ESD (CDM)	±1500	V
Latch_up	JEDEC78E Class I, $\pm100mA$	NA
Mechanical Shock	10000g@0.2ms half sine	NA

Note: Stress above those listed as 'Absolute Maximum Ratings' may cause permanent damage to the device. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

4 Pin Description

4.1 Pin Out View
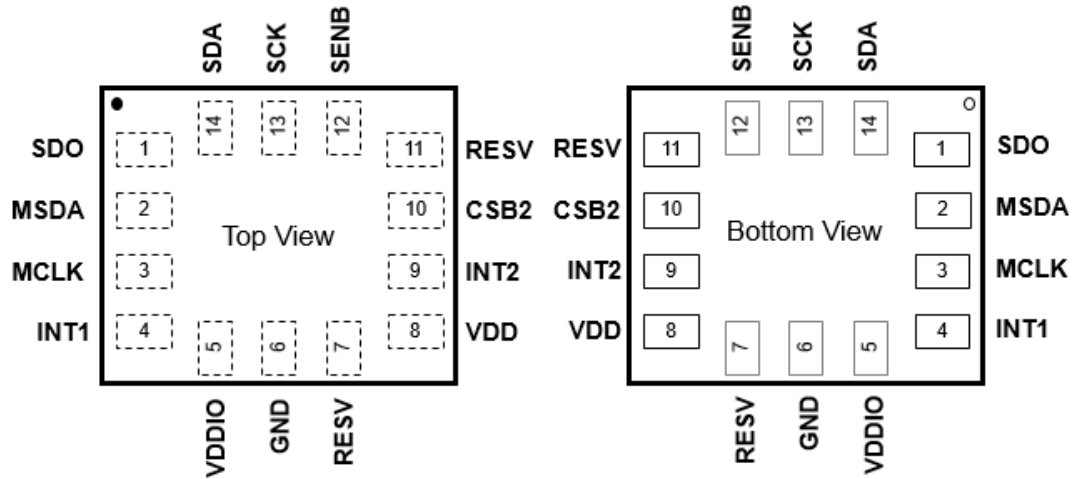
Figure 4: The pin out view of SH5001

4.2 Pin Descriptions

Table 9: Pin descriptions

Pin No.	Pin Name	Description
1	SDO	I^2C slave address LSB (A0), serial data output in SPI
2	MSDA	Auxiliary I^2C/ OIS interface serial data. Connect to external sensors or VDDIO.
3	MCLK	Auxiliary I^2C/ OIS interface serial clock. Connect to external sensors or VDDIO.
4	INT1	Interrupt digital output (push-pull or open-drain).
5	VDDIO	Digital I/O supply voltage.
6	GND	Ground for power supply.
7	RESV	No connect or connect to VDDIO or GND.
8	VDD	Power supply voltage and digital supply voltage.
9	INT2	Interrupt 1 digital output (push-pull or open-drain).
10	CSB2	Auxiliary SPI 3-wire interface enable.
11	RESV	No connect or connect to VDDIO or connect to GND.
12	SENB	I^2C/SPI (CSB) protocol select. 1: SPI idle mode/ I^2C communication enabled; 0: SPI communication mode/ I^2C disabled.
13	SCK	I^2C serial clock, SPI serial clock.
14	SDA	I^2C serial data, serial data input SDI in SPI.

5 Functional Explanations

5.1 6–Axis MEMS Sensor With 16-bit ADCs

SH5001 consists of a 3-axis angular rate sensor and a 3-axis acceleration sensor. It detects rotation and acceleration on the X, Y and Z axes. The resulting signal is amplified, demodulated, and filtered to produce a voltage that is proportional to the angular rate or the acceleration. For each axis an on-chip 16-bit ADC is used to digitize the output voltage. The full-range of the gyroscope is programmable at $\pm 125\, dps$, $\pm 250\, dps$, $\pm 500\, dps$, $\pm 1000\, dps$ and $\pm 2000\, dps$ and the full-range of the accelerometer is programmable at $\pm 2\, g$, $\pm 4\, g$, $\pm 8\, g$ and $\pm 16\, g$.

5.2 Digital Output Temperature Sensor

An on-chip temperature sensor is used to measure chip temperature of SH5001. The readings from the sensor can be read from the TEMP_DATA registers (0x0D[3:0] and 0x0C[7:0]) and the factory calibrated room temperature offset is stored in the ROOM_TEMP registers (0x2A[3:0]and 0x29[7:0]).

Both temperature readings and room temperature are 12-bit unsigned values and the temperature value can be converted to degrees centigrade by using the following formula:
Temperature (^oC) = (TEMP_DATA - ROOM_TEMP)/14 + 25

5.3 Quick Start Guide

This section gives some very basic application examples on how to configure the device.

5.3.1 Device Initialization

The initialization sequence of the device is shown in the following flow chart
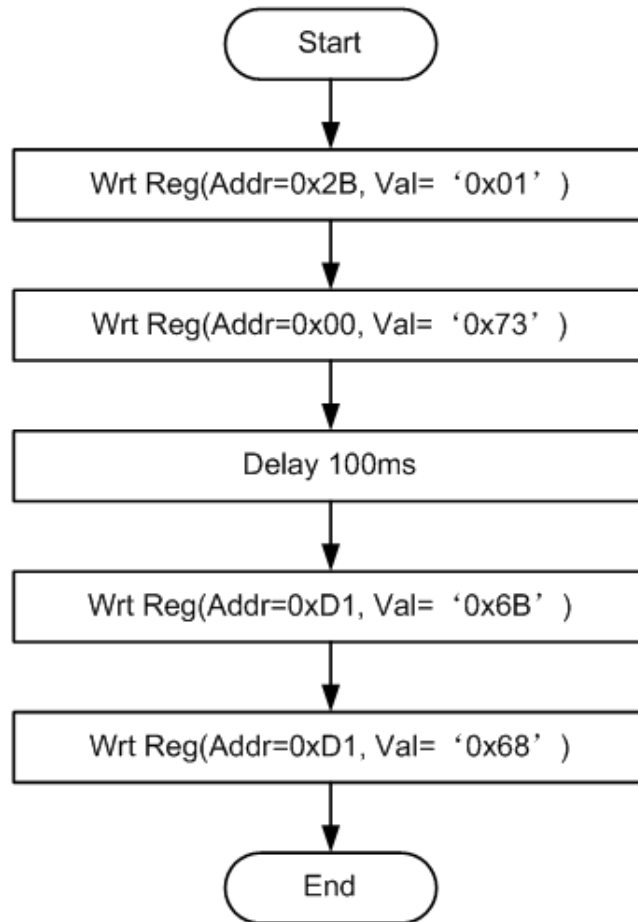
Figure 5: Initialization sequence of SH5001

5.3.2 Configuring The Device from Normal to Acc Only Mode

The following flow chart shows how to configure the device from normal mode to acc only mode.
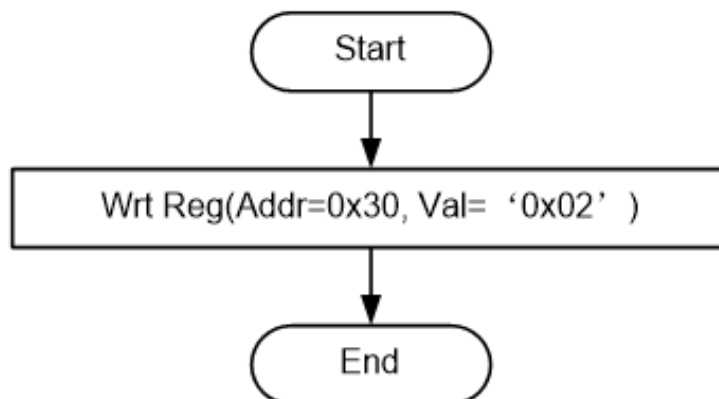
Figure 6: Configuring the device from normal to acc only mode

5.3.3 Configuring The Device from Normal to Acc Low Power Mode

The following flow chart shows how to configure the device from normal mode to acc low power mode.
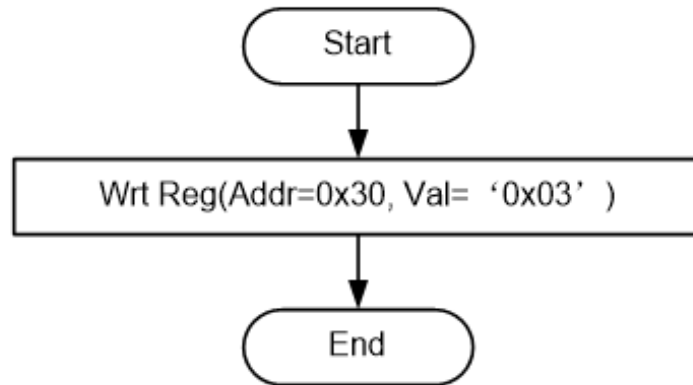
Figure 7: Configuring the device from normal to acc low power mode

5.3.4 Configuring The Device from Normal to Power Down Mode

The following flow chart shows how to configure the device from normal mode to acc low power mode.
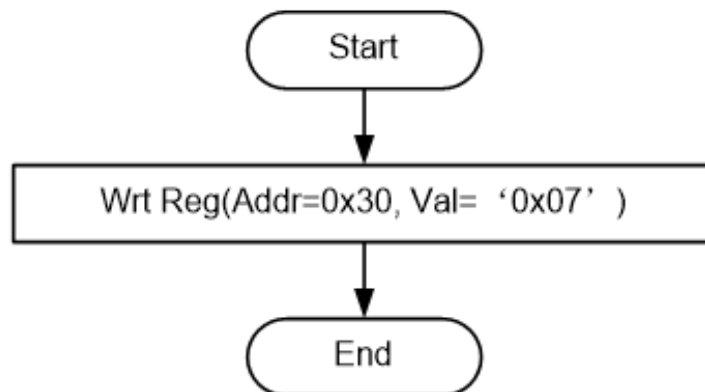
Figure 8: Configuring the device from normal to power down mode

5.3.5 Configuring The Device to Normal Modes

The following flow chart shows how to configure the device from other modes to normal mode.
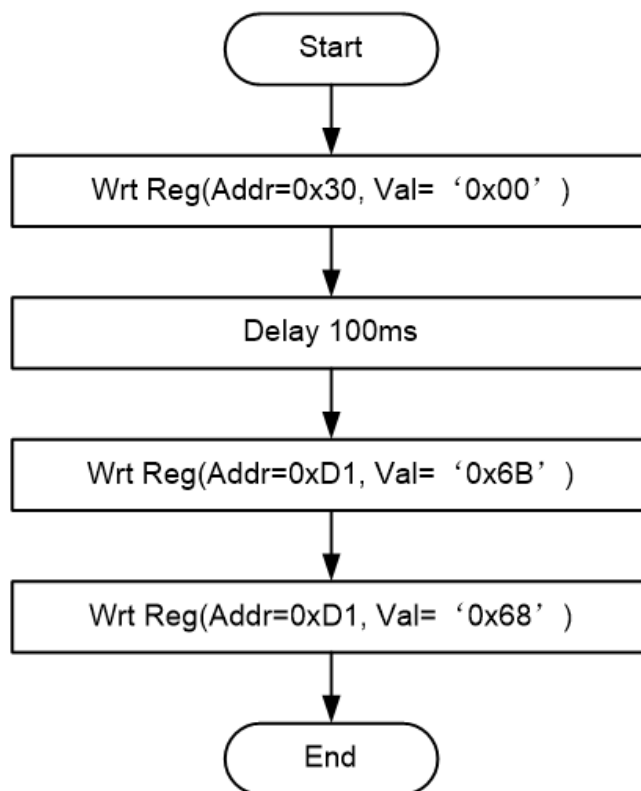
Figure 9: Configuring the device from other modes to normal mode

5.3.6 Configuring The Device to Gyro_only Modes

The following flow chart shows how to configure the device from other modes to gyro_only mode.
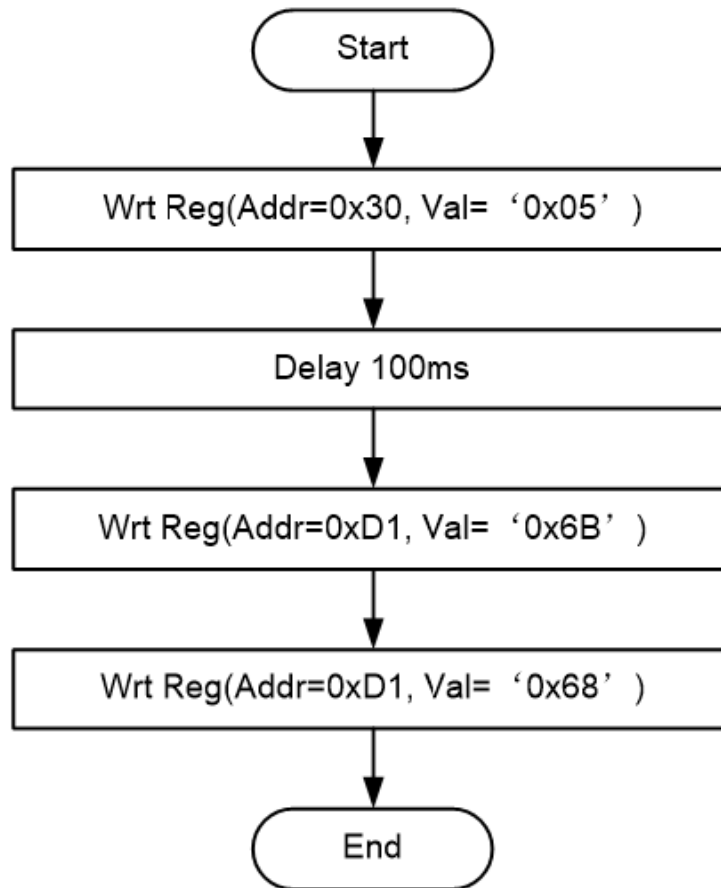
Figure 10: Configuring the device from other modes to gyro_only mode

5.4 FIFO

SH5001 contains a 2kB FIFO that is accessible via the serial interface. The FIFO configuration register determines which data is written into the FIFO. Possible choices include gyroscope data, accelerometer data, temperature readings,timestamps and auxiliary I^2C device input. Down sampling of both gyroscope and accelerometer data can be configured in register 0x39.

It can work in 4 modes determined by register 0x35[1:0].

Disable: FIFO is not operational and it remains empty.

FIFO Mode: Data from measurements are stored in FIFO. When the number of samples in FIFO equals the level specified in the watermark register (0x37[2:0] and 0x36[7:0]), the watermark interrupt is fired. FIFO continues to accumulate data until it is full and then stops collecting data. The watermark interrupt continues to occur until the number of samples in FIFO is less than the value stored in the watermark register.

Stream Mode: Data from measurements are stored in FIFO. When the number of samples in FIFO equals the level specified in the watermark register, the watermark interrupt bit is set. FIFO continues accumulating samples and holds the latest samples, discarding older data as new data arrives; The watermark interrupt continues to occur until the number of samples in FIFO is less than the value stored in the watermark register.

Trigger Mode: FIFO accumulates samples, holding the latest samples from measurements. After a trigger event occurs and an interrupt is sent, FIFO keeps the last n samples (where n is the value specified

by the watermark register) and then operates in FIFO mode, collecting new samples only when FIFO is not full.

Note that the FIFO data should be read first because setting the device into FIFO disable mode clears FIFO.

5.5 Interrupt

5.5.1 General Features

SH5001 contains 15 programmable interrupts and utilizes output pin INT1 or INT2 to send signal to an external microprocessor as an interrupt event occurs. Interrupts can be enabled or disabled by configuring interrupt control registers. The status register will be read by the external microprocessor to check the types of interrupt.

The interrupt pins can be set as either open-drain output or normal output by configuring register 0x42[3] for pin INT2 and 0x42[1] for pin INT1. When setting register value to '1' ('0'), the output pin is open-drain (normal) output. The active level of interrupt pins is determined by register 0x42[7]. By setting register 0x42[7] to '0'('1'), the active level of interrupt pins is high (low).

All the thresholds for interrupts are unsigned values.

Table 10: Interrupts supported by SH5001

Index	Interrupt Name	Enable	Flag
1	Inactivity Interrupt	0x40[5]	0x16[5] 0x19[7:4]
2	Activity Interrupt	0x40[4]	0x16[4] 0x19[7:4]
3	Double Tap Interrupt	0x40[3]	0x16[3] 0x19[3:0]
4	Single Tap Interrupt	0x40[2]	0x16[2] 0x19[3:0]
5	Tap Interrupt	0x40[2]/[3] 0x41[5]	0x17[4] 0x19[3:0]
6	Flat Interrupt	0x40[1]	0x16[1]
7	Orientation Interrupt	0x40[0]	0x16[0]
8	Free Fall Interrupt	0x41[0]	0x17[0]
9	Water Mark Interrupt	0x41[3]	0x17[3]
10	Gyro Data Ready Interrupt	0x41[2]	0x17[2]
11	Acc Data Ready Interrupt	0x41[1]	0x17[1]
12	Low-G Interrupt	0x40[7]	0x16[7] 0x18[0]
13	High-G interrupt	0x40[6]	0x16[6] 0x18[7:4]
14	SMD interrupt	0x41[4]	0x17[4]
15	Up-down interrupt	0x40[0] 0x44[7]	0x16[0]

5.5.2 Inactivity Interrupt

Inactivity detection uses consecutive acceleration values to detect lack of motion. Inactivity interrupt is enabled (disabled) by writing '1' ('0') to register 0x40[5]. if the slopes of all axes is lower than preset threshold defined by 0x57-0x59, and hold time is longer than that set in 0x5A, the interrupt is fired.

Each axis can be individually selected to participate in detecting inactivity. The axis participates the inactivity detection is determined by register 0x4D[2:0]. A setting of 0 excludes the selected axis from participation. If all axes are excluded, the function is disabled. For inactivity detection, all participating axes are logically AND, causing the inactivity function to trigger when all of the participating axes are less than the threshold for at least a period of time specified in register 0x5A.

The interrupt status is stored in register 0x16[5] and 0x19[7:4]. The inactivity interrupt supplies additional information about the detected inactivity. The axis that triggers the interrupt is indicated by register 0x19[6:4] that contains a value of '1'. The sign of the triggering slope is held in register 0x19[7] until the interrupt is retriggered. If register 0x19[7] = '0' ('1'), the sign is positive (negative).

5.5.3   Activity Interrupt

Activity detection uses consecutive acceleration values to detect changes in motion. Activity detection interrupt is enabled (disabled) by writing '1' ('0') to register 0x40[4].

The activity interrupt threshold is defined by register 0x54 and 0x55.

For activity detection, the acceleration value at the start of activity detection is taken as a reference value. New samples of acceleration are then compared to this reference value. If the magnitude of the difference exceeds the activity interrupt threshold, activity interrupt is fired.

Activity interrupt is generated only after a predefined number of consecutive acceleration values exceed the value defined by 0x56.

Each axis can be individually selected to participate in detecting activity. The axis participates activity detection is determined by register 0x4D[6:4]. A setting of '0' excludes the selected axis from participation. If all axes are excluded, the function is disabled. For activity detection, all participating axes are logically OR, causing the activity function to trigger when any of the participating axes exceeds the activity threshold for consecutive number of samples defined by register 0x56.

The interrupt status is stored in register 0x16[4]. The activity interrupt supplies additional information about the detected activity. The axis which triggers the interrupt is given by register 0x19[6:4] that contains a value of '1'. The sign of the triggering slope is held in register 0x19[7] until the interrupt is retriggered. If register 0x14[7] = '0' ('1'), the sign is positive (negative).

5.5.4   Double & Single Tap Interrupt

A tap event is detected if a pre-defined slope of the acceleration of at least one axis exceeds the threshold. Two different tap events are distinguished : a 'Single Tap' is a single event within a certain time and a 'Double Tap' consists of a single tap followed by a second event within a defined period of time.

- Step 1: The absolute value of an axis is more than preset threshold set by 0x4F and 0x50.

- Step 2: The large value last time should shorter than the period defined by 0x51; Single Tap is recognized, but need to prove no Double Tap.

- Step 3: Disable value comparator before the duration end which is set by 0x52.

- Step 4: Compare absolute value with threshold within the duration set by 0x53; If no large sample detected in this duration, Single Tap Interrupt is fired. Else go to Step 5.

- Step 5: If the large value last time is longer than the period defined by 0x51, Single Tap is proved. Otherwise, Double Tap is proved.

5.5.5   Tap Interrupt

Both Single Tap and Double Tap will cause Tap Interrupt.

5.5.6   Flat Interrupt

The flat detection feature gives information about the orientation of the device's z-axis relative to the g-vector. It recognizes whether the device is in a flat position or not. The flat angle θ is defined as:

$$\theta = atan(\sqrt{\frac{acc\_x^2 + acc\_y^2}{acc\_z^2}}) \tag{1}$$

in the above equation, acc_x, acc_y, acc_z are the x, y and z axis outputs of the accelerometer. If $acc\_x = acc\_y = 0$ and $acc\_z = 1g$, $\theta = 0$, indicating that the device is in a totally flat position. Similarly, the value of $8 \times tan^2\theta$ is compared with the threshold value defined by 0x4C[5:0] by the interrupt engine. If $8 \times tan^2\theta$ is less than the threshold and keeps enough time defined in 0x4C[7:6], Flat Interrupt is fired.

5.5.7   Orientation Interrupt

The orientation interrupt informs on an orientation change of the sensor with respect to the gravitational field vector g. There are the orientations upward/downward and orthogonal to that portrait upright, landscape left, portrait downside, and landscape right.

The sensor orientation is defined by the angles φ and θ (φ is rotation around the stationary z axis and θ is rotation around the stationary y axis). Therefore the magnitudes of the acceleration vectors are calculated as follows:

$$\begin{cases} acc\_x = 1g \times sin\theta \times cos\varphi \\ acc\_y = -1g \times sin\theta \times sin\varphi \\ acc\_z = 1g \times cos\theta \end{cases} \tag{2}$$

According to equation 2, if the outputs of three axes are given, the orientation angles are calculated as follows:

$$\begin{cases} \varphi = -atan(\frac{acc\_y}{acc\_x}) \\ \\ \theta = atan(\sqrt{\frac{acc\_x^2 + acc\_y^2}{acc\_z^2}}) \end{cases} \tag{3}$$

Depending on the value of orientation angles the orientation of the device in space is determined and stored in the orientation status register 0x16[0] . There are three orientation calculation modes: symmetrical, high-asymmetrical and low-asymmetrical. The mode is selected by the register 0x45[1:0].
The engine uses 16-bit acceleration data for the orientation recognition. For upside or downside orientation, 0x1A[2] has the definition:
$0 \rightarrow$ Upside $acc\_z > 0$
$1 \rightarrow$ Downside $acc\_z < 0$
Both portrait/landscape and upside/downside recognition use a hysteresis (*hyst*) which is decided by 0x4A and 0x4B. For each orientation mode, 0x45[1:0] has different meanings as shown in the following tables.

Table 11: Meaning of the orient mode register in symmetrical mode

Orient	Name	Condition	
00	Landscape left	$|acc\_y| < |acc\_x| - hyst$	& $acc\_x \geq 0$
01	Landscape right	$|acc\_y| < |acc\_x| - hyst$	& $acc\_x < 0$
10	Portrait upside down	$|acc\_y| > |acc\_x| + hyst$	& $acc\_y < 0$
11	Portrait upright	$|acc\_y| > |acc\_x| + hyst$	& $acc\_y \geq 0$

Table 12: Meaning of the orient mode register in high-asymmetrical mode

Orient	Name	Condition
00	Landscape left	$\|acc\_y\| < 2 \times (\|acc\_x\| - hyst) \quad \& \quad acc\_x \geq 0$
01	Landscape right	$\|acc\_y\| < 2 \times (\|acc\_x\| - hyst) \quad \& \quad acc\_x < 0$
10	Portrait upside down	$\|acc\_y\| > 2 \times \|acc\_x\| + hyst \quad \& \quad acc\_y < 0$
11	Portrait upright	$\|acc\_y\| > 2 \times \|acc\_x\| + hyst \quad \& \quad acc\_y \geq 0$

Table 13: Meaning of the orient mode register in low-asymmetrical mode

Orient	Name	Condition
00	Landscape left	$\|acc\_y\| < (\|acc\_x\| - hyst)/2 \quad \& \quad acc\_x \geq 0$
01	Landscape right	$\|acc\_y\| < (\|acc\_x\| - hyst)/2 \quad \& \quad acc\_x < 0$
10	Portrait upside down	$\|acc\_y\| > \|acc\_x\|/2 + hyst \quad \& \quad acc\_y < 0$
11	Portrait upright	$\|acc\_y\| > \|acc\_x\|/2 + hyst \quad \& \quad acc\_y \geq 0$

It is possible to block the Orientation Interrupt. The Orientation Interrupt blocking feature is configured via 0x45[3:2]. The value of '1.5g' is defined by 0x46 and 0x47. The value of the slope threshold is defined by 0x48 and 0x49.

The meaning of 0x45[3:2] is listed as follows:
'00': Orientation Interrupt blocking is disabled.
'01': Orientation Interrupt will be blocked if the device is close to the horizontal position or acceleration of any axis is larger than 1.5g.
'10': Orientation Interrupt will be blocked if the device is close to the horizontal position or acceleration of any axis is larger than 1.5g or the slope is larger than 0.2g.
'11': Orientation Interrupt will be blocked if the device is close to the horizontal position or the slope is larger than 0.4g or acceleration of any axis is larger than 1.5g or another orientation change is detected within 100ms.

5.5.8 FIFO Watermark Interrupt

Generate interrupt when FIFO data count is equal to the hold level defined in 0x37[2:0] and 0x36.

5.5.9 Gyroscope Data Ready Interrupt

Generate interrupt when gyroscope data is ready. If interrupt is not latched, INT1 can be consider as a clock signal with programmable duty cycle and right INT1_Length settings.

5.5.10 Accelerometer Data Ready Interrupt

Generate interrupt when accelerometer data is ready. If interrupt is not latched, INT1 can be consider as a clock signal with programmable duty cycle and right INT1_Length settings.

5.5.11 Free-fall Interrupt

Free-fall detection detects whether the device is falling. If the sum of absolute accelerations of all three axes $|acc\_x| + |acc\_y| + |acc\_z|$ is less than the threshold set by register 0x64 for a period longer than the value is specified in register 0x65, free-fall interrupt is generated. The free-fall interrupt is enabled (disabled) by writing '1' ('0') to register 0x41[0] and the interrupt status is stored in register 0x17[0].

The register 0x5E defines the threshold value. The meaning of register 0x5E depends on the range setting. The sum of absolute acceleration of all axes $|acc\_x| + |acc\_y| + |acc\_z|$ is compared with the value in register 0x5E to determine if a free-fall event occurred.

The register 0x5F defines the time value representing the minimum time that the value of all axes must be less than register 0x5E to generate a free-fall interrupt. The scale factor is 2ms/LSB. A value of 0 may result in undesirable behavior if the free-fall interrupt is enabled. Values between 100 ms and 350 ms (0x32 to 0xAF) are recommended.

5.5.12 Low-G Interrupt

Low-G interrupt is based on the comparison of acceleration data against a low-g threshold defined in 0x61 and 0x62. If the absolute values of the acceleration of all axes are lower than the threshold and last time is longer than the period defined in 0x63, Low-G interrupt is fired.

5.5.13 High-G Interrupt

High-G Interrupt is based on the comparison of acceleration data against a high-g threshold defined in 0x5E and 0x5F. If the absolute value of enabled axis is larger than the high-g threshold and last time is longer than the period defined in 0x60,High-G interrupt is fired .

5.5.14 Significant Motion Detection (SMD) Interrupt

- Step 1: First Motion Detection. This detection means the slope of any axis is above the *SMD_Thresh* defined by 0x5B and 0x5A.

- Step 2: Block Period. In this period defined by 0x5C[7:4], the SMD machine is waiting for the block period without any action.

- Step 3: Second Motion Detection. This detection means the slope of any axis is above the *SMD_Thresh* . If a second motion is detected, SMD interrupt will be set. If second motion is not detected before Proof Time Out defined by 0x5C[3:0], the SMD machine will be reset.
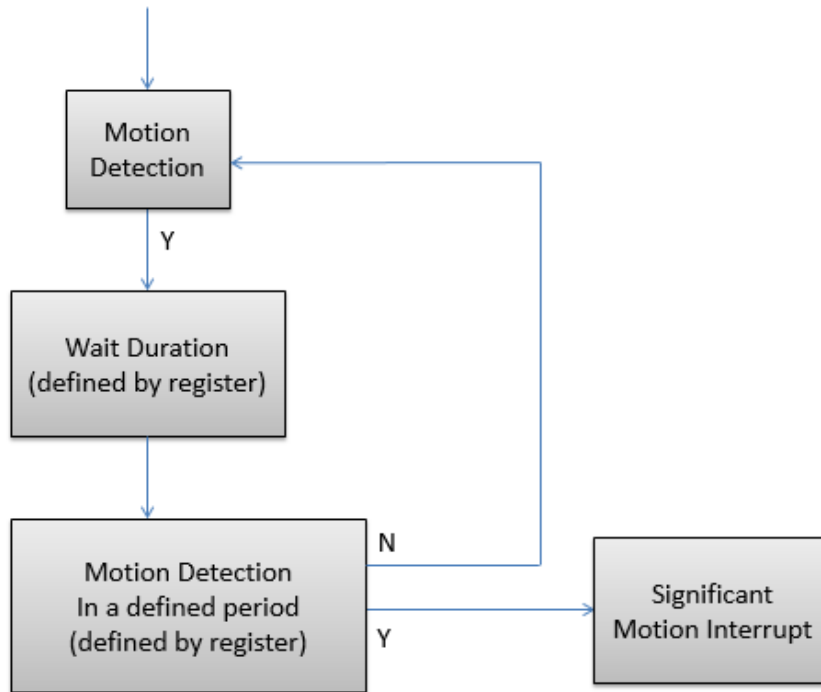
Figure 11: Block diagram of status

5.5.15   Up-Down Interrupt

Up-Down Interrupt is a special mode Orientation interrupt. When 0x44[7] is set to '1', Orient interrupt will work in up-down mode. Only up-down movement can be detected. The flag of this interrupt share the same flag of Orientation interrupt.

5.6   Fast Offset Compensation

Fast offset compensation offers an easy way to compensate the offset errors of gyroscope and accelerometer by setting the offset registers. It is convenient for "end-of-line trimming" with the customers device positioned in a well-defined orientation. Fast offset compensation is triggered by writing predefined values to 0x06. Gyroscope target value is always 0 dps, for accelerometer the target value depends on sensor position relative to the earth gravity field.

Position	Address	Value	Description
X (+1g)	0x06	0x90	Earth gravity filed is along the positive X axis
X (-1g)	0x06	0x91	Earth gravity filed is along the negative X axis
Y (+1g)	0x06	0x92	Earth gravity filed is along the positive Y axis
Y (-1g)	0x06	0x93	Earth gravity filed is along the negative Y axis
Z (+1g)	0x06	0x94	Earth gravity filed is along the positive Z axis
Z (-1g)	0x06	0x95	Earth gravity filed is along the negative Z axis

6 Digital Interfaces

6.1 General Description

SH5001 has both primary (I^2C and SPI configurable) and secondary interfaces. The secondary interface supports I^2C only. The secondary I^2C bus allows an external processor to act as master and communicates with the external device connected to the secondary I^2C bus pins (MSDA and MSCK). This is useful for configuring a magnetometer along with SH5001 to build a 9-DoF solution. In this mode, the secondary I^2C bus control logic of SH5001 is disabled, and the secondary I^2C pins MSDA and MSCK are connected to the main I^2C bus through analog switches.

The diagram below shows an application processor can communicate with an external digital output sensor connected to SH5001 through the auxiliary I^2C bus.

Figure 12: Connection diagram through the auxiliary I^2C bus

6.2 Primary Interfaces

By default, SH5001 operates in I^2C mode. It can also be configured to operate in SPI mode. I^2C and SPI digital interfaces share partly the same pins.

6.2.1 Primary Interface I^2C/SPI Protocol Selection

The protocol is automatically selected based on the chip select CSB pin behavior after power-up. At power-up, SH5001 is in I^2C mode. If CSB is connected to VDDIO during power-up and not changed then SH5001 works in I^2C mode. The interface switches from I^2C to SPI mode if a 'high' to 'low' transition happens on CSB pin.

6.2.2 Primary SPI Interface

The SPI interface of SH5001 is compatible with two modes, '00' (CPOL ='0' and CPHA='0') and '11' (CPOL ='1' and CPHA ='1'). The automatic selection between '00' and '11' is controlled based on the value of SCK after a falling edge of CSB. The page1 or page2 registers can be accessed by setting register 0x7F[0] to '0' or '1'.
The basic write, read and multiple write, read operations are illustrated in below waveforms.
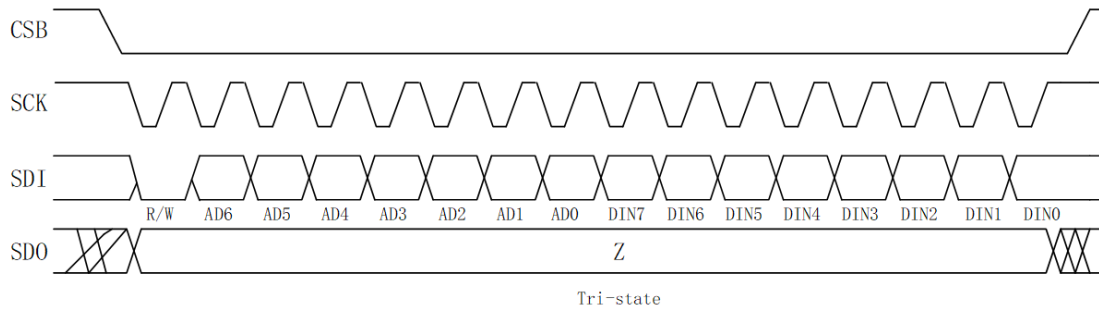
Figure 13: 4-wire SPI write sequence
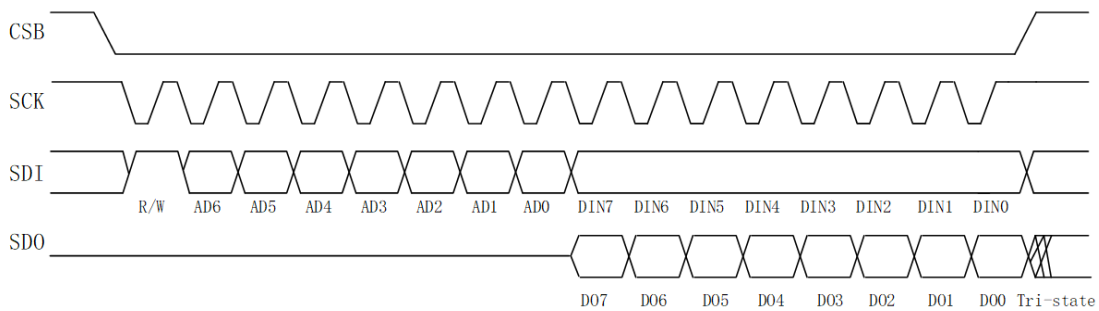
Figure 14: 4-wire SPI read sequence
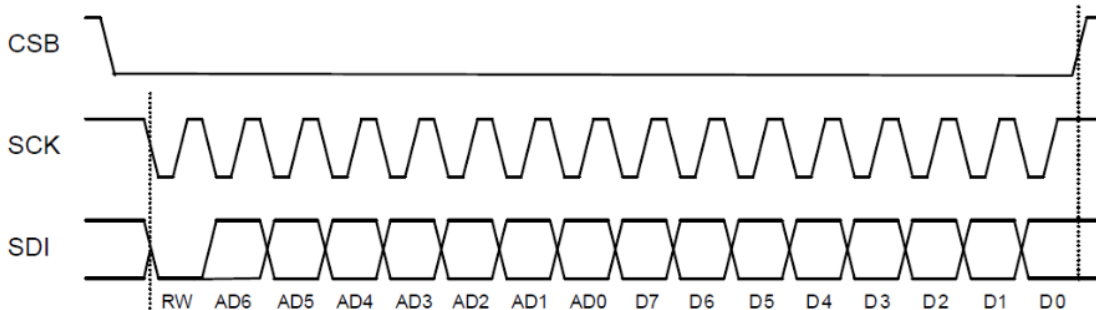
Figure 15: 3-wire SPI read and write sequence

The data bits shown in above waveforms are:

Bit[0]: Read/Write bit. When '0', the data SDI is written into the chip. When '1', the data SDO are read out from them chip.

Bit[1:7]: Address AD[6:0].

Bit[8:15]: In write mode, these are the data from SDI written into the address AD. In read mode, these are data read from the address AD.

Multiple read and write operations are done by keeping CSB low and continuing the data transaction and only the first address is written, addresses are automatically incremented internally as long as CSB stays active.

Multiple read and write are shown in figures below:
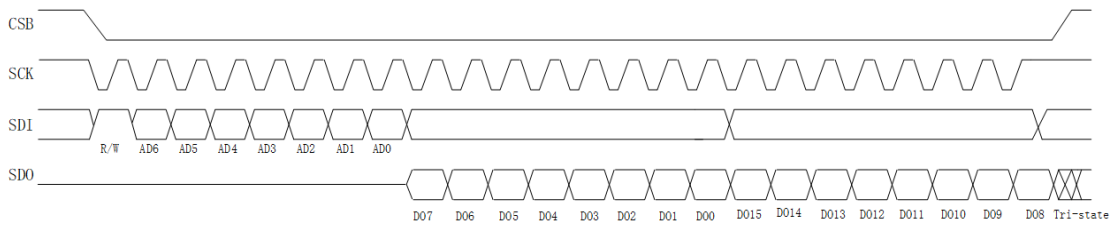
Figure 16: 4-wire SPI multiple read sequence
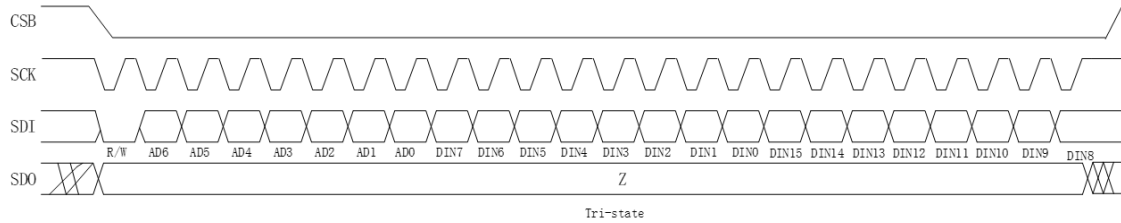
Figure 17: 4-wire SPI multiple write sequence

6.2.3 Primary I^{2}C Interface

The I^{2}C interface of SH5001 is a slave bus. There are two signals associated with the I^{2}C bus: the serial clock SCL and serial data SDA. The SDA is a bi-directional line used to send or receive data from the interface. Both lines must be connected to VDDIO through external pull-up resistors.

The default I^{2}C address of SH5001 is 0b0110110. It is used if the SDO pin is pulled to 'GND'. The alternative address 0b0110111 is selected by pulling SDO to 'VDDIO'.

The I^{2}C bus is implemented with both fast mode (400 kHz) and standard mode.

Data transfer with acknowledge is mandatory. The transmitter must release the SDA line during the acknowledge pulse. The receiver then must pull the SDA line 'low' so it remains low during the high period of the acknowledge clock pulse. A receiver which has been addressed is obliged to generate an acknowledge after each byte of data received.

The transaction begins with a start (ST) condition generated by master, followed by 7 bits slave address (SAD) and 1 read/write bit, then the master sends the one byte register address (RAD). If it is a read operation, a repeated start (SR) condition must be issued after the register address byte. If it is a write operation, the master will transmit data which will be written into the register addressed by register address byte. The slave sends out slave acknowledge condition (ACK) after the slave address issued by master matches its slave address, and after master sends out register address and receives data byte written by master. The master must assert master acknowledge condition (MACK) after receives data from slave.

Data are transferred in byte format with MSB sent out first. The number of bytes transferred is unlimited until no master acknowledge (MNACK) condition asserted by master for read operation, or when master issues stop condition for write operation.

Master	ST	SAD+W		RADR		DATA		SP
Slave			ACK		ACK		ACK	

Figure 18: I^{2}C single byte write

Master	ST	SAD+W		RADR		RS	SAD+R			MNACK	SP
Slave			ACK		ACK			ACK	DATA		

Figure 19: I^{2}C single byte read

Master	ST	SAD+W		RADR		DATA		DATA		SP
Slave			ACK		ACK		ACK		ACK	

Figure 20: I^{2}C multiple bytes write

Master	ST	SAD+W		RADR		RS	SAD+R			MACK		MNACK	SP
Slave			ACK		ACK			ACK	DATA		DATA		

Figure 21: I^{2}C multiple bytes read

6.3 Auxiliary I^{2}C Serial Interface

SH5001 contains an auxiliary I^{2}C bus which allows an external system processor to act as master and directly communicates to external sensors connected to the secondary I^{2}C bus pins (MSDA and MSCK) by setting 0xFD[3] to '1'. This is useful for configuring external devices, or for keeping SH5001 in a low-power mode. In this mode, the secondary I^{2}C bus control logic (third-party sensor interface block) of the SH5001 is disabled, and the secondary I^{2}C pins MSDA and MSCK are connected to the main I^{2}C bus through analog switches.

6.4 Auxiliary I^{2}C Interface

About OIS using,SH5001 set registers through UI SPI or I^{2}C. And get OIS data through OIS SPI.

The multiple read operations are illustrated in below waveform.
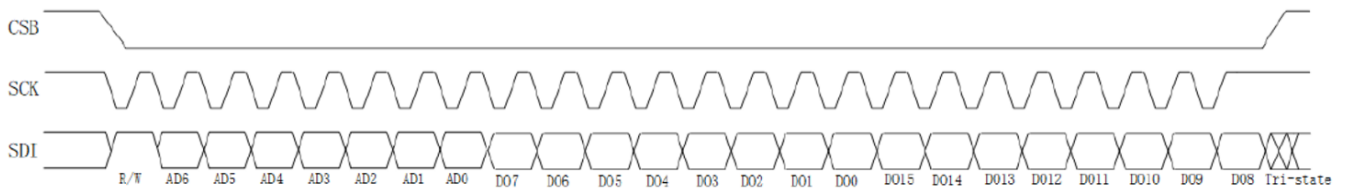
Figure 22: 3-wire SPI multiple read sequence

The specific steps are as follows:

- Step 1: Set register 0x2A to enable and config Time Stamp if needed.

- Step 2: Set register 0x27 to config OIS GYRO.

- Step 3: Set register 0x26 to config OIS ACC.

- Step 4:Set register 0x34[4:1] to enable OIS SPI.

- Step 5: Read register from 0x00 to 0x05 to get ACC data.

- Step 6: Read register from 0x06 to 0x0B to get GYRO data.

- Step 7: Read register from 0x0E to 0x10 to get Time Stamp data if needed.

7 Register Descriptions

7.1 Register Descriptions

7.1.1 Register 0x00-0x05: Accelerometer Data

Name: ACC_DATA_XL
Address: 0x00

Bit	Access	Default	Description
[7:0]	RO		Low 8 bits of ACC X-axis data. Write value'0x73' is an instruction for SoftReset but not operate the register actually.

Name: ACC_DATA_XH
Address: 0x01

Bit	Access	Default	Description
[7:0]	RO		High 8 bits of ACC X-axis data

Name: ACC_DATA_YL
Address: 0x02

Bit	Access	Default	Description
[7:0]	RO		Low 8 bits of ACC Y-axis data

Name: ACC_DATA_YH
Address: 0x03

Bit	Access	Default	Description
[7:0]	RO		High 8 bits of ACC Y-axis data

Name: ACC_DATA_ZL
Address: 0x04

Bit	Access	Default	Description
[7:0]	RO		Low 8 bits of ACC Z-axis data

Name: ACC_DATA_ZH
Address: 0x05

Bit	Access	Default	Description
[7:0]	RO		High 8 bits of ACC Z-axis data

7.1.2   Register 0x06-0x0B: Gyroscope Data

Name: GYRO_DATA_XL
Address: 0x06

Bit	Access	Default	Description
[7:0]	RO		Low 8 bits of GYRO X-axis data

Name: GYRO_DATA_XH
Address: 0x07

Bit	Access	Default	Description
[7:0]	RO		High 8 bits of GYRO X-axis data

Name: GYRO_DATA_YL
Address: 0x08

Bit	Access	Default	Description
[7:0]	RO		Low 8 bits of GYRO Y-axis data

Name: GYRO_DATA_YH
Address: 0x09

Bit	Access	Default	Description
[7:0]	RO		High 8 bits of GYRO Y-axis data

Name: GYRO_DATA_ZL
Address: 0x0A

Bit	Access	Default	Description
[7:0]	RO		Low 8 bits of GYRO Z-axis data

Name: GYRO_DATA_ZH
Address: 0x0B

Bit	Access	Default	Description
[7:0]	RO		High 8 bits of GYRO Z-axis data

7.1.3 Register 0x0C-0x0D: Temperature Data

Name: TEMP_DATA_L
Address: 0x0C

Bit	Access	Default	Description
[7:0]	RO		Low 8 bits of temperature data

Name: TEMP_DATA_H
Address: 0x0D

Bit	Access	Default	Description
[7:0]	RO		High 8 bits of temperature data

Name: INTERRUPT_STATUS_0_L
Address: 0x16

Bit	Access	Default	Description
7	RO	0	Log-G Interrupt Flag
6	RO	0	High-G Interrupt Flag
5	RO	0	In-Activity Interrupt Flag
4	RO	0	Activity Interrupt Flag
3	RO	0	Double Tap Interrupt Flag
2	RO	0	Single Tap Interrupt Flag
1	RO	0	Flat Interrupt Flag
0	RO	0	Orient Interrupt Flag

Name: INTERRUPT_STATUS_0_H
Address: 0x17

Bit	Access	Default	Description
7	RO	0	Reserved
6	RO	0	Reserved
5	RO	0	Tap Flag, Single Or Double Tap Interrupt Flag
4	RO	0	SMD Interrupt Flag
3	RO	0	FIFO Water-Mark Interrupt Flag
2	RO	0	Gyro Data Update Interrupt Flag
1	RO	0	ACC Data Update Interrupt Flag
0	RO	0	Free-Fall Interrupt Flag

Name: H-G&L-G_INTERRUPT_STATUS
Address: 0x18

Bit	Access	Default	Description
7	RO	0	High-G Sign
6	RO	0	High-G X-axis Interrupt Flag
5	RO	0	High-G Y-axis Interrupt Flag
4	RO	0	High-G Z-axis Interrupt Flag
3	RO	0	Reserved
2	RO	0	Reserved
1	RO	0	Reserved
0	RO	0	Low-G Interrupt Flag

Name: ACT-INA&TD_INTERRUPT_STATUS_REGISTER
Address: 0x19

Bit	Access	Default	Description
7	RO	0	ACT-INACT sign
6	RO	0	ACT-INACT X-axis Interrupt Flag
5	RO	0	ACT-INACT Y-axis Interrupt Flag
4	RO	0	ACT-INACT Z-axis Interrupt Flag
3	RO	0	TAP sign
2	RO	0	TAP X-axis Interrupt Flag
1	RO	0	TAP Y-axis Interrupt Flag
0	RO	0	TAP Z-axis Interrupt Flag

Name: ORIENT_STATUS
Address: 0x1A

Bit	Access	Default	Description
[7:3]	RO	00000	Reserved
[2:0]	RO	000	Orient status

Name: FIFO_STATUS_L
Address: 0x1B

Bit	Access	Default	Description
[7:0]	RO	00000000	FIFO count 7:0

Name: FIFO_STATUS_H
Address: 0x1C

Bit	Access	Default	Description
7	RO	0	Reserved
6	RO	0	Water mark status. 1: FIFO count is above water level. 0: FIFO count is below water level.
5	RO	0	FIFO Full flag. 1: True 0:False
4	RO	0	FIFO Empty flag. 1: True 0:False
[3:0]	RO	0000	FIFO count 11:8

Name: FIFO_READ_DATA_PORT
Address: 0x1D

Bit	Access	Default	Description
[7:0]	RO	00000000	FIFO data out. FIFO address will increase 1 when reading register18 one time. Burst FIFO read operation is supported.

Name:CHIP_ID
Address: 0x1F

Bit	Access	Default	Description
7	RO	1	Bit[7:5]: Chip family.
6	RO	0	001 – 'A'; 010 – 'B'; 011 – 'C';101 – 'K'
5	RO	1	
[4:1]	RO	0000	Bit[4:0]: Chip index.
0	RO	1	This chip ID '0xA1'means 'K01'

7.1.4   Register 0x20-0x23: Accelerometer Configurations

Name:ACC_CONFIG_0
Address: 0x20

Bit	Access	Default	Description
7	RW	0	Sniff mode. 1 : Enable. 0 : Disable In this mode, down sample rate is 1/1520
[6:2]	RW	00000	Reserved
1	RW	0	Bypass LPF in digital ACC. 1: Enable. 0: Disable
0	RW	0	ACC digital filter enable. 1: Enable. 0 : Disable

Name:ACC_CONFIG_1
Address: 0x21

Bit	Access	Default	Description
7	RW	0	Reserved
[6:4]	RW	000	ACC range configuration. 000: 2g; 001: 4g; 010: 8g; 011: 16g 100: 32g; 101: Reserved; 110: Reserved; 111: Reserved
[3:0]	RW	0000	ACC ODR configuration. Refer to Table 14

Table 14: ACC ODR Selector

0x21[3:0]	ODR(Hz)	0x21[3:0]	ODR(Hz)	0x21[3:0]	ODR(Hz)	0x21[3:0]	ODR(Hz)
0000	1000	0100	Reserved	1000	2000	1100	Reserved
0001	500	0101	Reserved	1001	4000	1101	Reserved
0010	250	0110	Reserved	1010	8000	1110	Reserved
0011	125	0111	Reserved	1011	Reserved	1111	Reserved

Name:ACC_CONFIG_2
Address: 0x22

Bit	Access	Default	Description
[7:4]	RW	000	Reserved
[3:0]	RW	0000	ACC LPF coefficient configuration. The cutoff frequency is ODR*N. N refer to Table 15

Table 15: ACC cutoff frequency factor

0x22[3:0]	N	0x22[3:0]	N	0x22[3:0]	N	0x22[3:0]	N
0000	0.40	0100	0.24	1000	0.12	1100	0.04
0001	0.36	0101	0.20	1001	0.10	1101	0.03
0010	0.32	0110	0.16	1010	0.08	1110	0.02
0011	0.28	0111	0.14	1011	0.06	1111	0.01

7.1.5 Register 0x23-0x27 Gyroscope Configurations

Name:GYRO_CONFIG_1
Address: 0x23

Bit	Access	Default	Description
[7:2]	RW	000000	Reserved
1	RW	0	GYRO low-pass filter bypass. 1: Enable. 0: Disable
0	RW	0	GYRO digital filter enable. 1: Enable. 0: Disable

Name: GYRO_CONFIG_2
Address: 0x24

Bit	Access	Default	Description
7	RW	0	Reserved
6	RW	0	GYRO range configurations.
5	RW	0	000: 31; 001:62; 010: 125; 011: 250
4	RW	0	100: 500; 101: 1000; 110: 2000; 111: Reserved
[3:0]	RW	0000	GYRO ODR configurations. Refer to Table 16

Table 16: GYRO scope ODR configurations

0x24[3:0]	ODR(Hz)	0x24[3:0]	ODR(Hz)	0x24[3:0]	ODR(Hz)	0x24[3:0]	ODR(Hz)
0000	1000	0100	Reserved	1000	2000	1100	Reserved
0001	500	0101	Reserved	1001	4000	1101	Reserved
0010	250	0110	Reserved	1010	8000	1110	Reserved
0011	125	0111	Reserved	1011	16000	1111	Reserved

Name: GYRO_CONFIG_3
Address: 0x25

Bit	Access	Default	Description
[7:4]	RW		Reserved
[3:0]	RW	0000	GYRO LPF cutoff frequency configurations. The cutoff frequency is ODR*N. N refer to Table 17

Table 17: GYRO cutoff frequency factor

0x25[3:0]	N	0x25[3:0]	N	0x25[3:0]	N	0x25[3:0]	N
0000	0.40	0100	0.24	1000	0.12	1100	0.04
0001	0.36	0101	0.20	1001	0.10	1101	0.03
0010	0.32	0110	0.16	1010	0.08	1110	0.02
0011	0.28	0111	0.14	1011	0.06	1111	0.01

7.1.6 Register 0x24-0x27 OIS Configurations

Name: ACC_OIS_CONFIG
Address: 0x26

Bit	Access	Default	Description
7	RW	0	ACC OIS enable.　　　　　　　　　1: Enable. 0: Disable
6	RW	0	ACC OIS range configuration.
5	RW	0	000: 2g. 001: 4g. 010: 8g. 011: 16g.
4	RW	0	100: 32g. 101:Reserved. 110: Reserved. 111: Reserved.
3	RW	0	ACC OIS LPF cutoff frequency configuration.
2	RW	0	00: Disable. 01: 0.02*ODR. 10: 0.04*ODR. 11: 0.08*ODR.
1	RW	0	ACC OIS ODR configuration.
0	RW	0	00: 1kHz. 01: 2kHz. 10: 4kHz. 11: 8kHz.

Name: GYRO_OIS_CONFIG
Address: 0x27

Bit	Access	Default	Description
7	RW	0	GYRO OIS enable.　　　　　　　　1: Enable. 0: Disable
6	RW	0	GYRO OIS range configurations.
5	RW	0	000: 31. 001: 62. 010: 125. 011: 250.
4	RW	0	100: 500. 101: 1000. 110:2000. 111: Reserved.
3	RW	0	GYRO OIS LPF configurations.
2	RW	0	00: bypass LPF. 01: 0.02*ODR. 10: 0.04*ODR. 11: 0.08*ODR.
1	RW	0	GYRO OIS ODR configurations.
0	RW	0	00: 1kHz. 01: 2kHz. 10: 4kHz. 11: 8kHz.

Name: TEMP_CONFIG_1
Address: 0x29

Bit	Access	Default	Description
[7:0]	RW	00000000	Room temperature 7:0

Name: TEMP_CONFIG_2/TIME_STAMP_CONFIG
Address: 0x2A

Bit	Access	Default	Description
7	RW	0	Reserved
6	RW	0	Time Stamp enable. 1: Enable. 0: Disable
5	RW	0	Time Stamp ODR selector. 1: 25kHz. 0: 1kHz
4	RW	0	Reserved
3	RW	0	Room temperature 11:8
2	RW	0	
1	RW	0	
0	RW	0	

Name: AGC_CONFIG_1
Address: 0x2B

Bit	Access	Default	Description
7	RW	0	CVA Max-Gain use set value. 1: set value; 0: AGC
6	RW	0	CVA Max-Gain set value.
5	RW	0	PGA Max-Gain use set value. 1: set value; 0: AGC
4	RW	0	PGA Max-Gain set value.
3	RW	0	Reserved
2	RW	0	AGC clock inverter enable. 1: inverted; 0: input clock.
1	RW	0	AGC BPF bypass. 1: bypass BPF. 0: use BPF.
0	RW	0	AGC disable. 1: reset Digital AGC. 0: normal AGC.

Name: I^{2}C&SPI_CONFIG
Address: 0x34

Bit	Access	Default	Description
[7:6]	RW	00	Reserved
5	RW	0	UI SPI 3-wire mode enable. 0: 4-wire mode. 1: 3-wire mode
4	RW	0	OIS SPI enable. 1: Enable. 0: Disable
[3:0]	RW	0000	Reserved

Name: FIFO_CONFIG
Address: 0x35

Bit	Access	Default	Description
7	RW	0	FIFO reset. 1: Reset. 0: Normal
[6:2]	RW	00000	Reserved
1	RW	0	FIFO mode selector.
0	RW	0	00 : No FIFO.01: FIFO mode 10: Stream Mode. 11: Trig mode.

Name: FIFO_WATER_MARK_LEVEL_L
Address: 0x36

Bit	Access	Default	Description
[7:0]	RW	00000000	FIFO water mark level

Name: FIFO_WATER_MARK_LEVEL_H
Address: 0x37

Bit	Access	Default	Description
7	RW	0	Reserved
6	RW	0	Time Stamp.
5	RW	0	Master I^{2}C Z.
4	RW	0	Master I^{2}C Y.
3	RW	0	Reserved
2	RW	0	FIFO water mark level 10:8
1	RW	0	
0	RW	0	

Name: FIFO_CHANNEL_ENABLE_L
Address: 0x38

Bit	Access	Default	Description
7	RW	0	MI^{2}C X.
6	RW	0	TEMP.
5	RW	0	GYRO Z.
4	RW	0	GYRO Y.
3	RW	0	GYRO X.
2	RW	0	ACC Z.
1	RW	0	ACC Y.
0	RW	0	ACC X.

Name: FIFO_SUBSAMPLE_CONFIG
Address: 0x39

Bit	Access	Default	Description
7	RW	0	ACC FIFO subsample enable.　　　　　1: Enable. 0: Disable
6	RW	0	ACC FIFO subsample ratio.
5	RW	0	000 : 1/2. 001 : 1/4. 010 : 1/8. 011 : 1/16.
4	RW	0	100 : 1/32. 101 : 1/64. 110 : 1/128. 111 : 1/256.
3	RW	0	Gyro FIFO subsample enable.　　　　1: Enable. 0: Disable
2	RW	0	Gyro FIFO subsample ratio.
1	RW	0	000 : 1/2. 001 : 1/4. 010 : 1/8. 011 : 1/16.
0	RW	0	100 : 1/32. 101 : 1/64. 110 : 1/128. 111 : 1/256.

Name: MASTER_I^{2}C_CONFIG
Address: 0x3A

Bit	Access	Default	Description
7	RW	0	MI^{2}C function reset.　　　　　　　1: Reset. 0: Normal
6	RW	0	MI^{2}C auto read mode. 1: MI^{2}C will read slave device reg0 $\sim$ reg6 auto. 0: Manual mode.
5	RO	0	MI^{2}C operation failure flag
4	RO	0	MI^{2}C operation success flag
3	RW	0	Reserved
2	RW	0	
1	RW	0	MI^{2}C work when in manual mode. Auto clear. 1: Work. 0: Idle
0	RW	0	MI^{2}C read operation.　　　　1: Read operation. 0: Write

Name: MI^{2}C_CONFIG_2
Address: 0x3B

Bit	Access	Default	Description
7	RW	0	Reserved
6	RW	0	
5	RW	0	MI^{2}C auto read mode ODR.
4	RW	0	00 : 200Hz. 01: 100Hz. 10: 50Hz. 11: 25Hz
[3:0]	RW	0000	MI^{2}C operation speed selector (N). (1MHz/(6+3*N)). When N is 0, MI^{2}C frequency is 166KHz. When N is 15, MI^{2}C frequency is 19.6KHz.

Name: MI^{2}C_COMMAND
Address: 0x3C

Bit	Access	Default	Description
[7:1]	RW	0000000	Slave I^{2}C device address
0	RW	0	Reserved

Name: MI^{2}C_COMMAND_2
Address: 0x3D

Bit	Access	Default	Description
[7:0]	RW	00000000	Operation command/reg-address of slave I^{2}C device.

Name: MI^{2}C_WRITE_DATA
Address: 0x3E

Bit	Access	Default	Description
[7:0]	RW	00000000	Data writing to slave I^{2}C device.

Name: MI^{2}C_READ_DATA
Address: 0x3F

Bit	Access	Default	Description
[7:0]	RO	00000000	Data reading from slave I^{2}C device.

Name: TNTERRUPT_ENABLE_L
Address: 0x40

Bit	Access	Default	Description	
7	RW	0	Low-G Interrupt Enable.	1: Enable. 0: Disable
6	RW	0	High-G Interrupt Enable.	1: Enable. 0: Disable
5	RW	0	Inactivity Interrupt Enable.	1: Enable. 0: Disable
4	RW	0	Activity Interrupt Enable.	1: Enable. 0: Disable
3	RW	0	Double Tap Interrupt Enable.	1: Enable. 0: Disable
2	RW	0	Single Interrupt Enable.	1: Enable. 0: Disable
1	RW	0	Flag Interrupt Enable.	1: Enable. 0: Disable
0	RW	0	Orient Interrupt Enable.	1: Enable. 0: Disable

Name: INTERRUPT_ENABLE_H
Address: 0x41

Bit	Access	Default	Description	
[7:5]	RW	000	Reserved	
4	RW	0	SMD Interrupt enable.	1: Enable. 0: Disable
3	RW	0	FIFO WaterMark Interrupt Enable.	1: Enable. 0: Disable
2	RW	0	Gyro Data Ready Interrupt Enable.	1: Enable. 0: Disable
1	RW	0	ACC Data Ready Interrupt Enable.	1: Enable. 0: Disable
0	RW	0	Free Fall Interrupt Enable.	1: Enable. 0: Disable

Name: INTERRUPT_CONFIG
Address: 0x42

Bit	Access	Default	Description	
7	RW	0	The polarity of INT2.	1: Low. 0: High
6	RW	0	INT1 auto clear. 1: INT1 auto clear after period defined in 0x45. 0: INT1 clear by reading interrupt status.	
5	RW	0	The polarity of INT2.	
4	RW	0	Interrupt flag clear mode. 1: Clear interrupt status by any register read operation 0: Clear interrupt status by reading the register.	
[3:2]	RW	00	INT2 open mode. 00: No output. 01: Push pull 10: Open drain. 11: Push pull	
[1:0]	RW	00	INT1 open mode. 00: No output. 01: Push pull 10: Open drain. 11: Push pull	

Name: INT1_LENGTH
Address: 0x43

Bit	Access	Default	Description
[7:0]	RW	00000000	INT1 length when auto-clear mode. The count compared with INT1 length is clock of 512Hz.

Name: ORIENT_INTERRUPT_CONFIG_0
Address: 0x44

Bit	Access	Default	Description
7	RW	0	Reserved
6	RW	0	Up-down orient INT1 disable. 1: Disable. 0: Enable
[5:0]	RW	000000	Theta for flat recognition and orient blocking.

Name: ORIENT_INTERRUPT_CONFIG_1
Address: 0x45

Bit	Access	Default	Description
[7:4]	RW	0000	Reserved
3	RW	0	Orient INT1 blocking mode.
2	RW	0	00: No blocking. 01: Theta blocking or acceleration in any axis >1.5g. 10: Theta block or acceleration slope in any axis >0.2g or acceleration in any axis >1.5g. 11: The blocking or acceleration slope in any axis >0.4g or acceleration in any axis >1.5g and value of orient is not stable for at least 100ms.
1	RW	0	Orient mode. 00/11: Symmetrical.
0	RW	0	01: High-asymmetrical. 10: Low-asymmetrical

Name: ORIENT_1.5g_VALUE_L
Address: 0x46

Bit	Access	Default	Description
[7:0]	RW	00000000	1.5g value low 8-bit. For orient blocking use.

Name: ORIENT_1.5g_VALUE_H
Address: 0x47

Bit	Access	Default	Description
[7:0]	RW	00000000	1.5g value high 8-bit. For orient blocking use.

Name: ORIENT_SLOPE_L
Address: 0x48

Bit	Access	Default	Description
[7:0]	RW	00000000	Slope value low 8-bit. For orient blocking use.

Name: ORIENT_SLOPE_H
Address: 0x49

Bit	Access	Default	Description
[7:0]	RW	00000000	Slope value high 8-bit. For orient blocking use.

Name: ORIENT_HYST_VALUE_L
Address: 0x4A

Bit	Access	Default	Description
[7:0]	RW	00000000	HYST value low 8-bit. For orient blocking use.

Name: ORIENT_HYST_VALUE_H
Address: 0x4B

Bit	Access	Default	Description
[7:0]	RW	00000000	HYST value high 8-bit. For orient blocking use.

Name: FLAT_CONFIG
Address: 0x4C

Bit	Access	Default	Description
[7:6]	RW	00	Flat time threshold. When flat_cnt is over flat_limit, flat status will be recognized. flat_limit will be: 00: 512. 01: 1024. 10: 2048. 11: Reserved.
[5:0]	RW	000000	Flat theta.

Name: ACT_INACT_CONFIG
Address: 0x4D

Bit	Access	Default	Description
7	RW	0	Reserved
6	RW	0	Axis-X ACT enable. 1: Enable. 0: Disable
5	RW	0	Axis-Y ACT enable. 1: Enable. 0: Disable
4	RW	0	Axis-Z ACT enable. 1: Enable. 0: Disable
3	RW	0	Reserved
2	RW	0	Axis-X INACT enable. 1: Enable. 0: Disable
1	RW	0	Axis-Y INACT enable. 1: Enable. 0: Disable
0	RW	0	Axis-Z INACT enable. 1: Enable. 0: Disable

Name: ACT_INACT_CONFIG_2/TAP_AXIS_SELECTOR
Address: 0x4E

Bit	Access	Default	Description
7	RW	0	Act/In-ACT clear. 1: Clear.0: Normal
6	RW	0	Reserved
5	RW	0	Reserved
4	RW	0	Reserved
3	RW	0	TAP axis-X enable. 1: Enable. 0: Disable
2	RW	0	TAP axis-Y enable. 1: Enable. 0: Disable
1	RW	0	TAP axis-Z enable. 1: Enable. 0: Disable
0	RW	0	ACT-INACT link. 0: No link. 1: Link ACT-INACT.

Name: TAP_THRESHOLD_L
Address: 0x4F

Bit	Access	Default	Description
[7:0]	RW	00000000	Threshold 7:0 For TAP Interrupt.

Name: TAP_THRESHOLD_H
Address: 0x50

Bit	Access	Default	Description
[7:5]	RW	000	Reserved
[4:0]	RW	00000	Threshold 12:8 For TAP Interrupt.

Name: TAP_DURATION
Address: 0x51

Bit	Access	Default	Description
[7:0]	RW	00000000	TAP Duration. Count by 1KHz clock.

Name: TAP_LATENCY
Address: 0x52

Bit	Access	Default	Description
[7:0]	RW	00000000	TAP latency. Count by 1KHz clock.

Name: DOUBLE_TAP_WINDOW
Address: 0x53

Bit	Access	Default	Description
[7:0]	RW	00000000	Double TAP window. Count by 512Hz clock. If the second TAP occurs out of the window, double TAP will not be recognized.

Name: ACT_THRESHOLD_L
Address: 0x54

Bit	Access	Default	Description
[7:0]	RW	00000000	ACT threshold 7:0. If any of SlopeX or SlopeY or SlopeZ is more than this threshold, ACT can be recognized.

Name: ACT_THRESHOLD_H
Address: 0x55

Bit	Access	Default	Description
[7:0]	RW	00000000	ACT threshold high.

Name: ACT_TIME
Address: 0x56

Bit	Access	Default	Description
[7:0]	RW	00000000	ACT recognition time. Count by ODR set by 0x21. When the value is more than threshold and keep enough time longer than ACT time, ACT can be recognized.

Name: INACT_THRESHOLD_L
Address: 0x57

Bit	Access	Default	Description
[7:0]	RW	00000000	INACT threshold low 8-bit. When all axis ACC slope is less than this threshold, INACT can be recognized.

Name: INACT_THRESHOLD_H
Address: 0x58

Bit	Access	Default	Description
[7:0]	RW	00000000	INACT threshold high 8-bit. When all axis ACC slope is less than this threshold, INACT can be recognized.

Name: INACT_TIME
Address: 0x59

Bit	Access	Default	Description
[7:0]	RW	00000000	INACT recognition time. Count by 1Hz clock. When the value is more than threshold and keep enough time longer than INACT time, INACT can be recognized.

Name: SMD_THRESHOLD_L
Address: 0x5A

Bit	Access	Default	Description
[7:0]	RW	00000000	SMD threshold low 8-bit. If the slope of any axis is more than this threshold for the first time. And after the block time, within the proof time, the slope is also more than the threshold. Then SMD interrupt is detected.

Name: SMD_THRESHOLD_H
Address: 0x5B

Bit	Access	Default	Description
[7:0]	RW	00000000	SMD threshold high 8-bit. If the slope of any axis is more than this threshold for the first time. And after the block time, within the proof time, the slope is also more than the threshold. Then SMD interrupt is detected.

Name: SMD_TIME_CONFIG
Address: 0x5C

Bit	Access	Default	Description
[7:4]	RW	0000	SMD block time selector. The block time (s),refer to table 18
[3:0]	RW	0000	SMD proof time selector. The proof time (s),refer to table 19

Table 18: Block time

0x5C[3:0]	N	0x5C[7:4]	N	0x5C[B:8]	N	0x5C[F:C]	N
0000	0.5	0100	3	1000	0	1100	12
0001	1	0101	4	1001	8	1101	14
0010	1.5	0110	5	1010	9	1110	15
0011	2	0111	6	1011	10	1111	16

Table 19: Proof time

0x5C[3:0]	Len	0x5C[7:4]	Len	0x5C[B:8]	Len	0x5C[F:C]	Len
0000	0.2	0100	0.5	1000	0.9	1100	1.8
0001	0.25	0101	0.6	1001	1.0	1101	2.1
0010	0.3	0110	0.7	1010	1.2	1110	2.4
0011	0.4	0111	0.8	1011	1.5	1111	2.8

Name: HIGHG_LOWG_CONFIG
Address: 0x5D

Bit	Access	Default	Description	
7	RW	0	HighG all axis enable.	1: Enable. 0: Disable
6	RW	0	Axis-X highG enable.	1: Enable. 0: Disable
5	RW	0	Axis-Y highG enable.	1: Enable. 0: Disable
4	RW	0	Axis-Z highG enable.	1: Enable. 0: Disable
[3:1]	RW	000	Reserved	
0	RW	0	LowG all axis enabe.	1: Enable. 0: Disable

Name: HIGHG_THRESHOLD_L
Address: 0x5E

Bit	Access	Default	Description
[7:0]	RW	00000000	HighG threshold 7:0. ACC absolute value/8 compares with the threshold. If the value is more than threshold, highG can be recognized.

Name: HIGHG_THRESHOLD_H
Address: 0x5F

Bit	Access	Default	Description
[7:5]	RW	000	Reserved
[4:0]	RW	00000	HighG threshold 12:8. ACC absolute value/8 compares with the threshold. If the value is more than threshold, highG can be recognized.

Name: HIGHG_TIME
Address: 0x60

Bit	Access	Default	Description
[7:0]	RW	00000000	HighG Time. Count by 512Hz clock. If the value is more than threshold and cycle count is more than HighG time, HighG can be recognized.

Name: LOWG_THRESHOLD_L
Address: 0x61

Bit	Access	Default	Description
[7:0]	RW	00000000	LowG threshold 7:0. ACC absolute value/8 compares with the threshold. If the value of every axis is less than threshold, lowG can be recognized.

Name: LOWG_THRESHOLD_H
Address: 0x62

Bit	Access	Default	Description
[7:5]	RW	000	Reserved
[4:0]	RW	00000	LowG threshold 12:8. ACC absolute value/8 compares with the threshold. If the value of every axis is less than threshold, lowG can be recognized.

Name: LOWG_TIME
Address: 0x63

Bit	Access	Default	Description
[7:0]	RW	00000000	LowG Time. Count by 512Hz clock. If the value is less than threshold and cycle count is more than lowG time, lowG can be recognized.

Name: FREE-FALL_THRESHOLD
Address: 0x64

Bit	Access	Default	Description
[7:0]	RW	00000000	FreeFall threshold. The sum of all axis absolute value/8 compares with the threshold. If the value is less than threshold, Free-Fall can be recognized.

Name: FREE-FALL_TIME
Address: 0x65

Bit	Access	Default	Description
[7:0]	RW	00000000	Free-Fall Time. Count by 512Hz clock. If the value is less than threshold and cycle count is more than Free-Fall time, Free-Fall can be recognized.

Name: INTERRUPT_INT1/INT2_LOCATION_SELECTOR_L
Address: 0x66

Bit	Access	Default	Description	
7	RW	0	Low-G Interrupt Location.	1: INT2. 0: INT1
6	RW	0	High-G Interrupt Location.	1: INT2. 0: INT1
5	RW	0	Inactivity Interrupt Location.	1: INT2. 0: INT1
4	RW	0	Activity Interrupt Location.	1: INT2. 0: INT1
3	RW	0	Double Tap Interrupt Location.	1: INT2. 0: INT1
2	RW	0	Single Interrupt Location.	1: INT2. 0: INT1
1	RW	0	Flat Interrupt Location.	1: INT2. 0: INT1
0	RW	0	Orient Interrupt Location.	1: INT2. 0: INT1

Name: INTERRUPT_INT1/INT2_LOCATION_SELECTOR_H
Address: 0x67

Bit	Access	Default	Description	
7	RW	0	Reserved	
6	RW	0	Reserved	
5	RW	0	TAP Interrupt Location.	1: INT2. 0: INT1
4	RW	0	SMD Interrupt Location.	1: INT2. 0: INT1
3	RW	0	FIFO WaterMark Interrupt Location.	1: INT2. 0: INT1
2	RW	0	Gyro Data Update Interrupt Location.	1: INT2. 0: INT1
1	RW	0	ACC Data Update Interrupt Location.	1: INT2. 0: INT1
0	RW	0	Free Fall Interrupt Location.	1: INT2. 0: INT1

Name: ADC_CONFIG
Address: 0xD1

Bit	Access	Default	Description	
[7:5]	RW	011	ADC bias current_1 trim	
[4:2]	RW	010	ADC bias current_2 trim	
1	RW	0	ADC1 reset control bit.	1:Reset adc.0:Normal work.
0	RW	0	ADC2 reset control bit.	1:Reset adc.0:Normal work.

Name: TEST_PIN_SELECTOR_AND_MI^{2}C_BYPASS
Address: 0xFD

Bit	Access	Default	Description
[7:4]	RW	0000	Reserved
3	RW	0	MI^{2}C BYPASS enable. 1: Skip the internal controller,connect SCL to MSCK and SDA to MSDA directly. 0: Internal controller of MI^{2}C operates MSDA and MSCK.
[2:0]	RW	000	Reserved

Name: I^{2}C_SLAVE_DEVICE_ADDRESS
Address: 0xFF

Bit	Access	Default	Description
7	RW	0	Reserved
6	RW	0	
[5:0]	RW	000000	I^{2}C Slave device address high 7:2. I^{2}C slave device address bit 1 is decided by external pin MISO when I^{2}C mode is selected. I^{2}C slave device address bit 0 is R/W operation bit.

8 Application Hints

8.1 Orientation of Axes

The diagram below shows the orientation of the axes of sensitivity and the polarities of rotation. Note the pin1 marker in the figure.
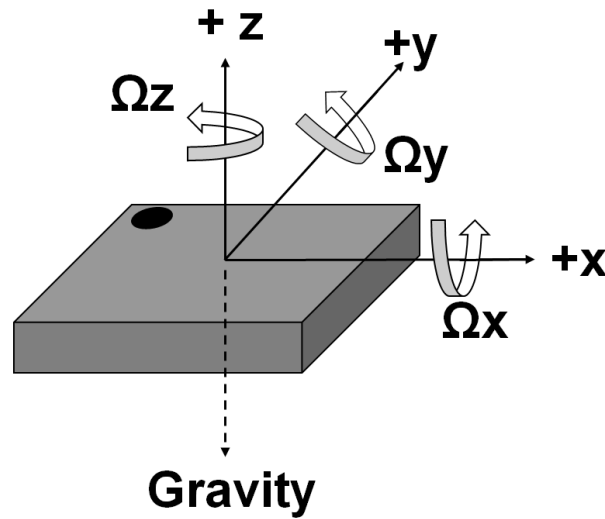
Figure 23: Orientation of axes sensitivity and polarity of rotation

8.2 Typical Application Circuits
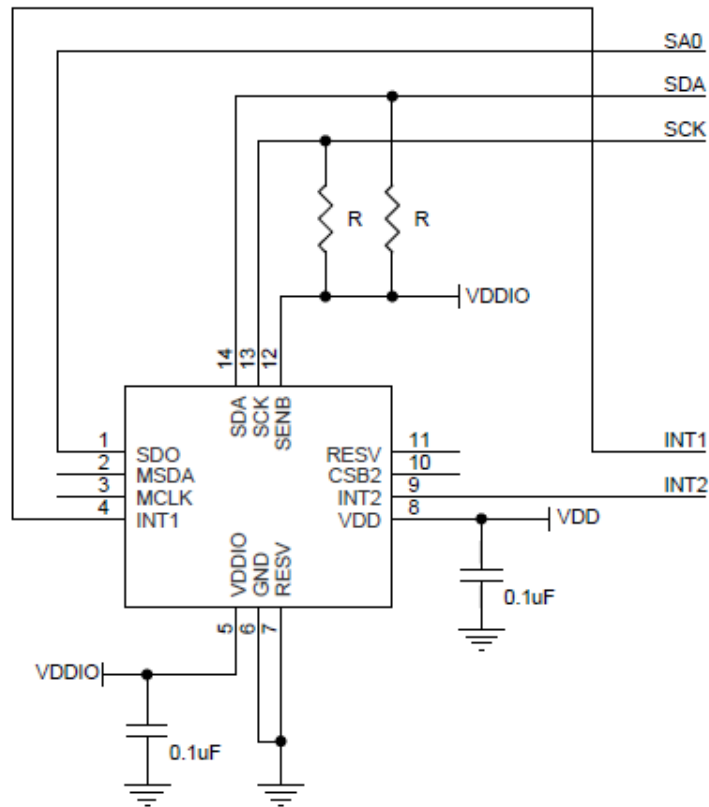
Figure 24: Reference application circuitry using only primary I^{2}C interface
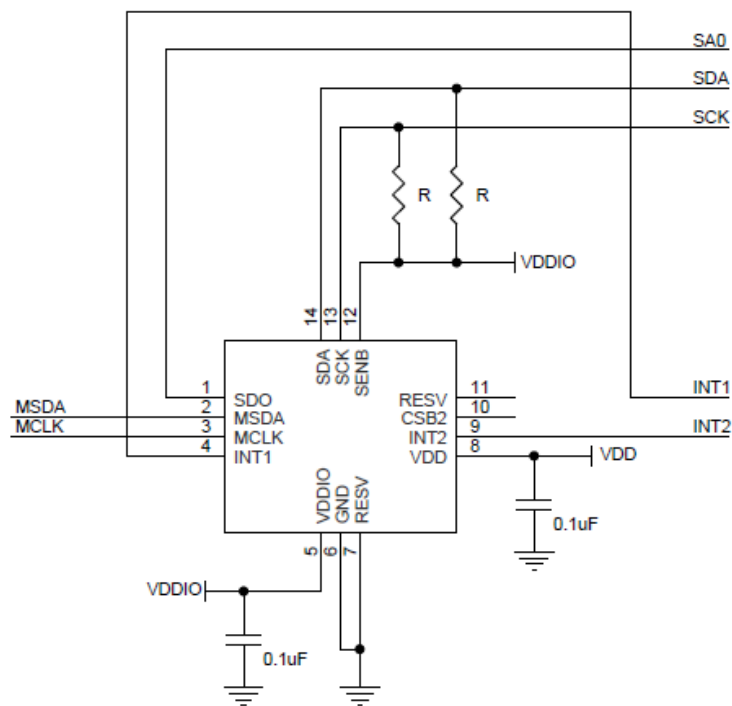
Figure 25: Reference application circuitry using primary and secondary I^{2}C interface
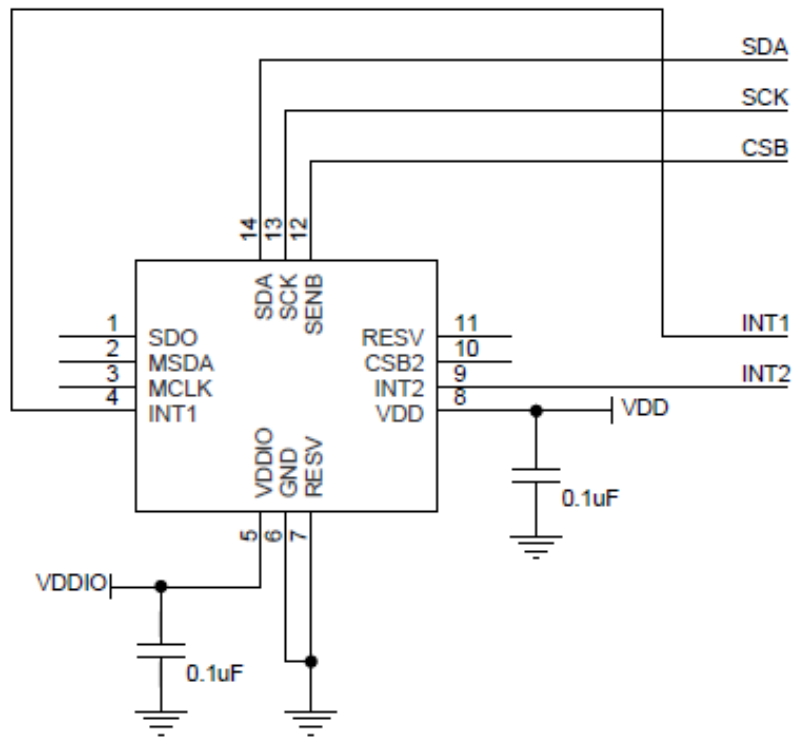
Figure 26: Reference application circuitry using SPI 3-wire interface
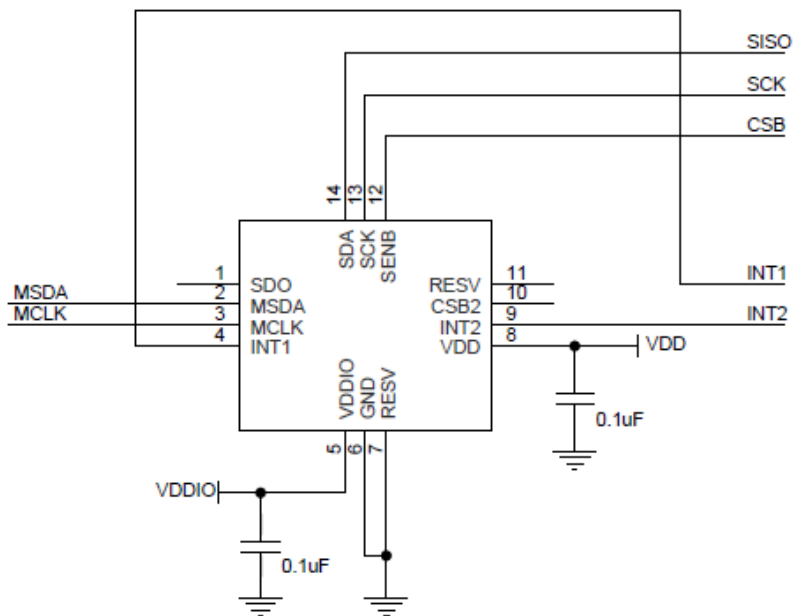
Figure 27: Reference application circuitry using SPI 3-wire and secondary I^{2}C interface
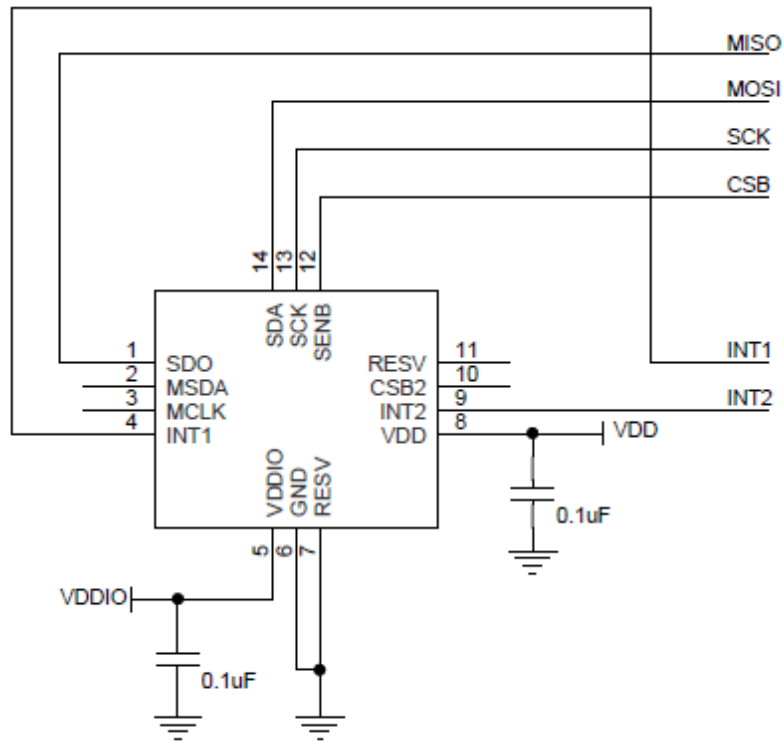
Figure 28: Reference application circuitry using SPI 4-wire interface
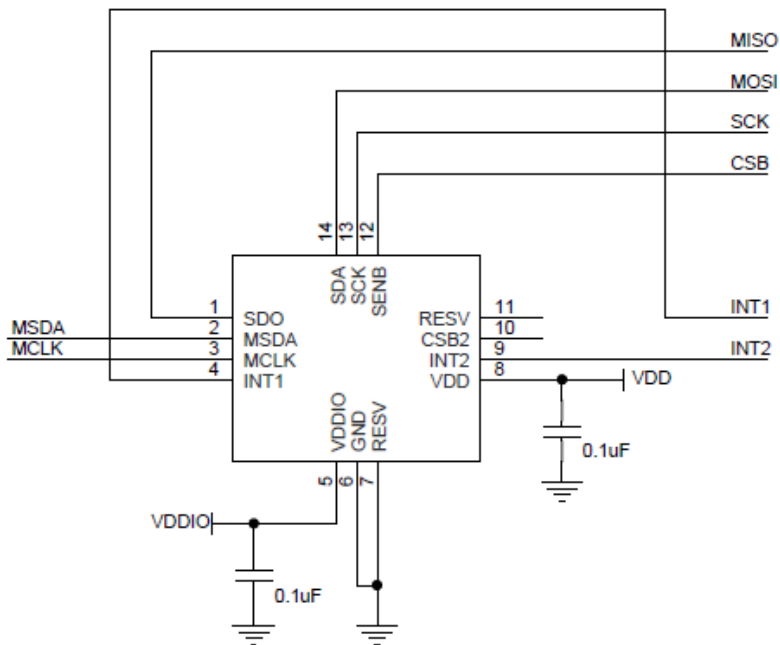
Figure 29: Reference application circuitry using SPI 4-wire and secondary I^{2}C interface
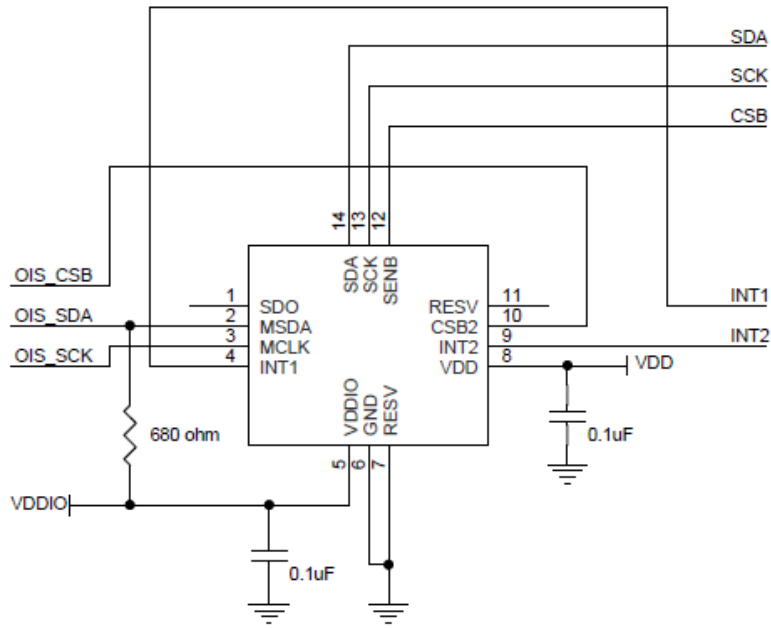
Figure 30: Reference application circuitry using UI SPI 3-wire and OIS SPI 3-wire interface
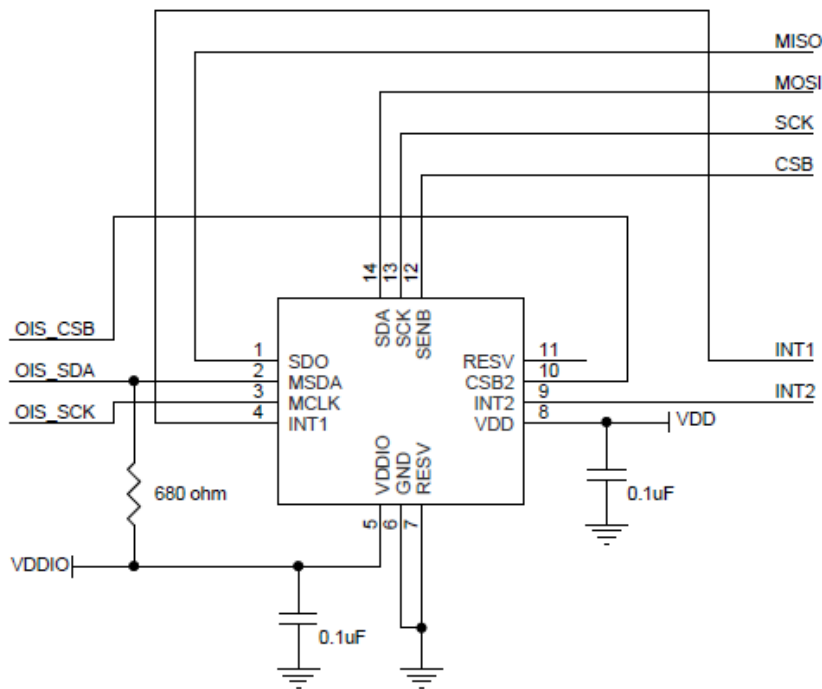
Figure 31: Reference application circuitry using UI SPI 4-wire and OIS SPI 3-wire interface
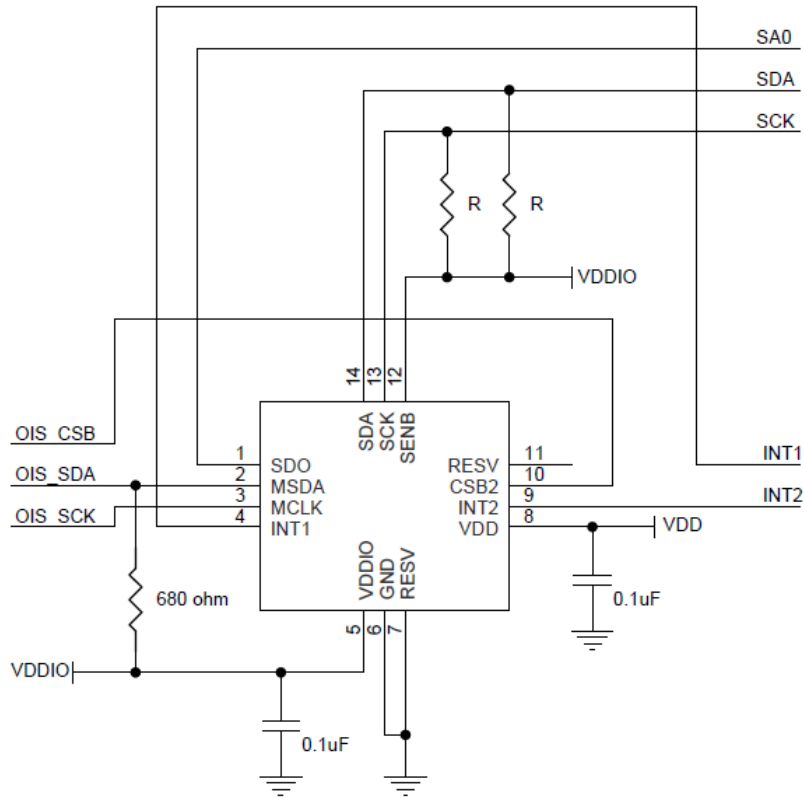
Figure 32: Reference application circuitry using UI I^{2}C and OIS SPI 3-wire interface
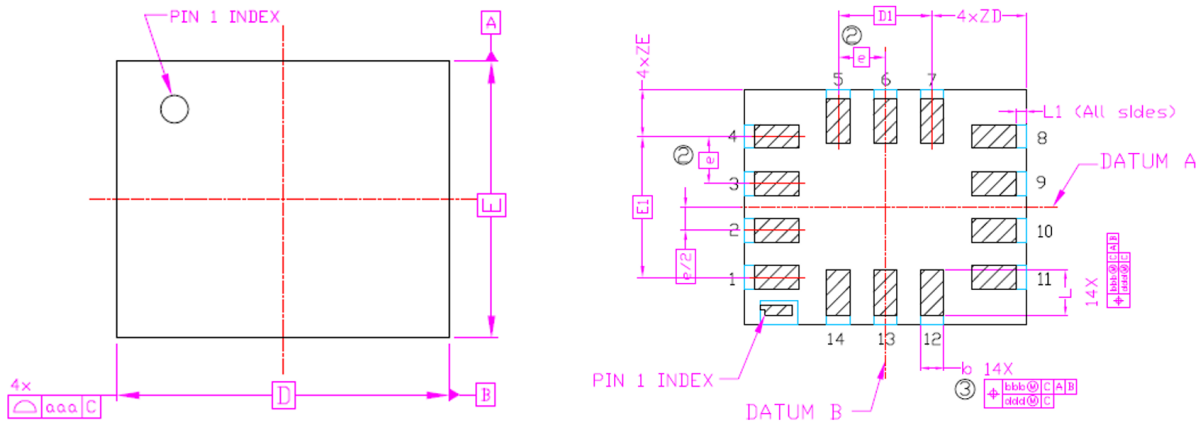
8.3 Package Information

8.3.1 Device Outline Dimensions
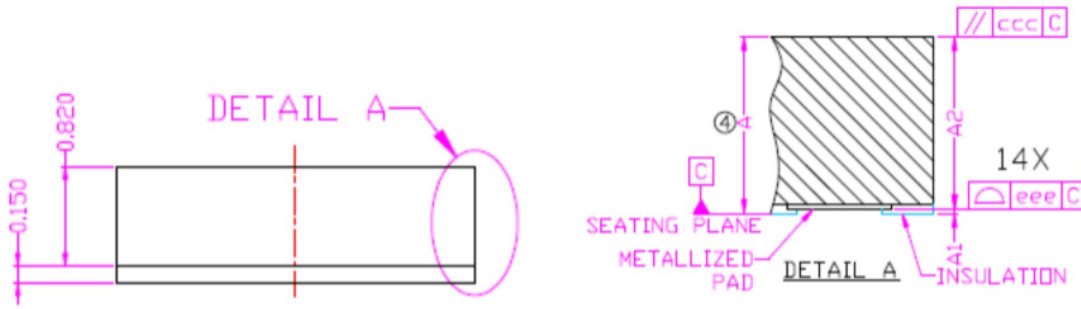

Figure 33: Top & bottom view of the device

Figure 34: Side view of the device

Table 20: Dimension references (unit: *mm*)

Ref	Min	Typ	Max	Ref	Min	Typ	Max
A	0.93	0.99	1.05	D1		1.00 BSC	
A1			0.03	E1		1.50 BSC	
A2			1.02	ZD		1.00 BSC	
b	0.2	0.25	0.3	ZE		0.50 BSC	
L	0.425	0.475	0.525	e		0.50 BSC	
D	2.90	3.00	3.10	L1	0.00	0.10	0.20
E	2.40	2.50	2.60				

Note: The dimensional tolerance of `aaa`, `bbb` and `ccc` is 0.10 *mm* and that of `ddd` and `eee` is 0.08 *mm*.

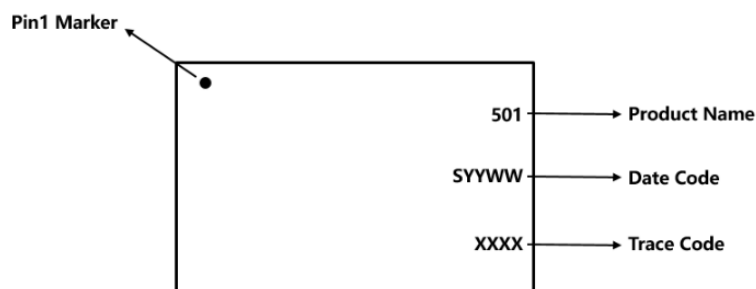### 8.3.2 Package Laser Mark

Figure 35: Package laser mark

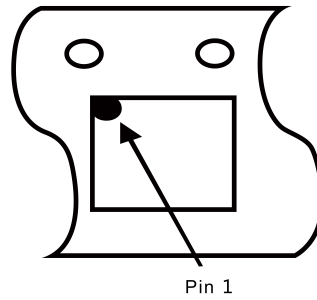### 8.3.3 Packaging Direction

Figure 36: Packaging direction
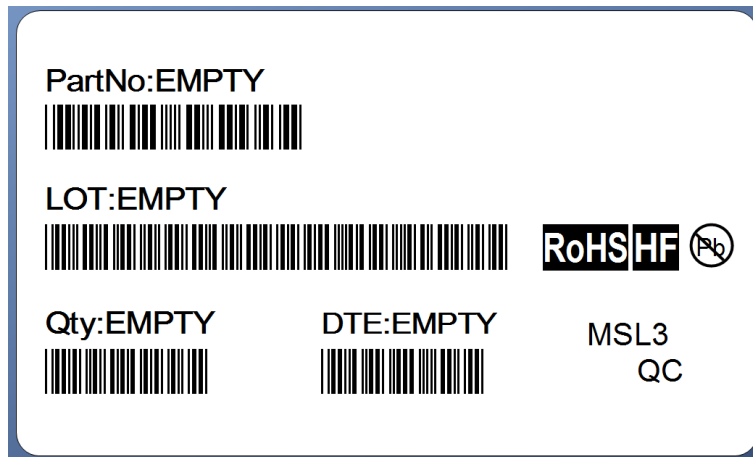
8.3.4 Packaging Label

Figure 37: Packaging label example

8.3.5 Packaging of Product

Figure 38: Packaging of the product

8.4 Soldering Guidelines

The device fulfils the lead-free soldering requirements of the IPC/JEDEC J-STD-020 Pb-free standard. Reflow soldering with a peak temperature T_p of 260^oC.
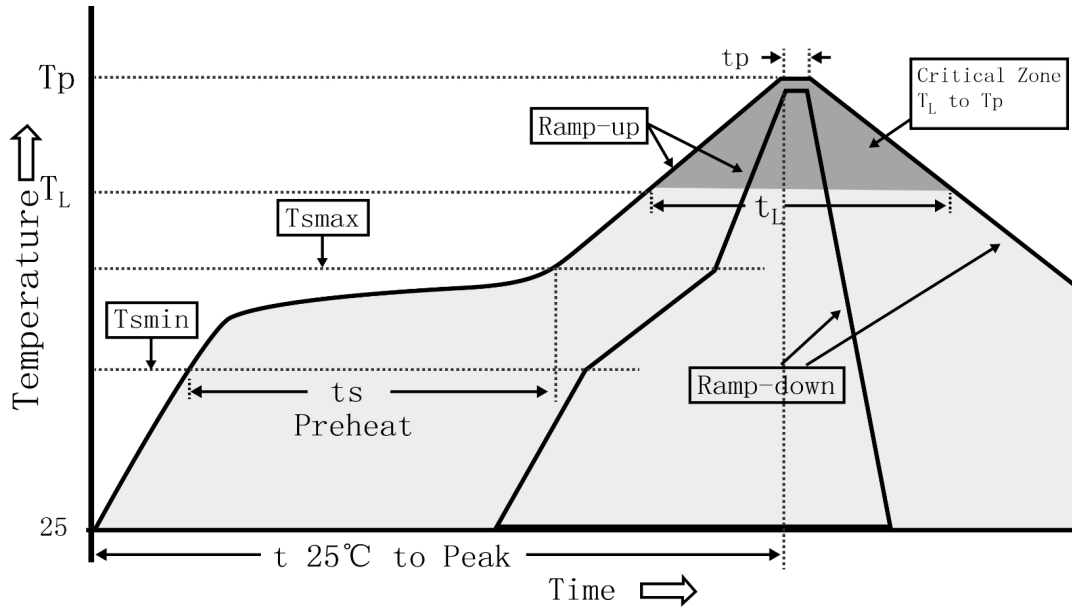

Figure 39: Recommended soldering reflow condition

Table 21: Recommended soldering reflow condition

Profile Feature	Pb-free Assembly
Average ramp-up rate (Ts_{max} to T_p)	$3\,^oC/s$ max
Preheat	
- Temperature Min (Ts_{min})	$150\,^oC$
- Temperature Max (Ts_{max})	$200\,^oC$
- Time (Ts_{min} to Ts_{max}) (ts)	$60 - 80\,s$
Time maintained above:	
- Temperature (T_L)	$217\,^oC$
- Time (t_L)	$60 - 150\,s$
Peak Temperature (T_p)	$260\,^oC$
Time within 5 ^oC of actual Peak Temperature	$20 - 40\,s$
Ramp-down rate	$6\,^oC/s$ max
Time 25 ^oC to Peak Temperature	8 min max

8.5 Storage Condition

The storage condition follows JEDEC J-STD-020, MSL3.

9 Reliability

9.1 Reliability Standard

SH5001 reliability test plan follows JEDEC 47I standards, 'Stress-Test-Driven Qualification of Integrated Circuits'.

10 Environment Compliant

SH5001 is compliant with RoHS 2.0 standards and meet HF requirements.

11 Disclaimer

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12   Revision History

Date	Revision	Changes
2022-08-25	1.0	Preliminary version